

DESIGN AND IMPLEMENTATION OF A REPEATER FOR ETHERNET

*A Thesis Submitted
in Partial Fulfilment of the Requirements
for the Award of the Degree of*

MASTER OF TECHNOLOGY

by

SQN LDR A D NARAYAN

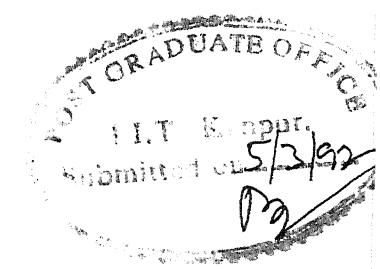
to the

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY KANPUR

MARCH 1992

CERTIFICATE



*This is to certify that this work entitled
DESIGN AND IMPLEMENTATION
OF A REPEATER FOR ETHERNET
by Sqn Ldr A D Narayan has been carried
out under my supervision and has not been submitted
elsewhere for the award of a degree.*

K R Srivathsan

Dr. K R SRIVATHSAN

Asst. Professor

**Department of Electrical Engineering
Indian Institute of Technology Kanpur**

11 MAY 1992

CENTRAL LIBRARY

See No. A113360

EE-1992-M-NAR-DES

113360

To

THE ALMIGHTY

WHO IS NOT VISIBLE BUT AVAILABLE AROUND US

सर्व धर्मान् परिव्यज्य मामेकं शारणं ब्रज
अहं त्वा सर्वं पापैर्मयौ मोक्षाग्निष्ठामि मा शुचः

ACKNOWLEDGEMENT

I wish to express my deep gratitude to my guide Dr K R Srivathsan whose guidance enabled me to undertake and finish this nice little challenging project, which was undertaken by one B Tech student one year back and he was partially successful. Dr K R Srivathsan, whose brain child was this, was always in look for a better solution which must work as a field model and finally his able guidance fulfilled this requirement. I also express my gratitude to Dr R N Biswas who had helped me in knowing the intricacies of this project in absence of Dr K R Srivathsan.

I am also grateful to research engineers of ERNET project Mr Sameer Dubey, Mr Mallikarjuna and Mr Nagendra Goel who helped me in setting up the test bench and obliged me with their experiences of software and hardware.

I am also thankful to Mr Bhatnagar, Mr K K Shukla and Mr R N Pal who helped me in getting the required components and necessary test equipments time to time.

At the last but not the least I am indebted to Venkatesh who inspite of his own work load of his Ph.D thesis could find some time to help me at the fag end of my thesis in giving a beautiful facelift to this write up.

Finally my sincere thanks goes to my wife Mily who always inspired me and encouraged me towards fulfilling the requirements of this project. She always shown me her smiling face when ever I was late to go home, inspite of the trouble she used to have due to my naughty but loving daughters Runjhun and Payal and the burden of home front in my absence.

Sqn Ldr A D Narayan

TABLE OF CONTENTS

CHAPTER 1	INTRODUCTION	1
1.1	Computer Network	1
1.2	Standards For Networks	2
1.2.1	Open System Interconnection	2
1.2.2	IEEE 802 Series	5
1.3	IEEE 802.3 Standard	6
1.3.1	Physical Layer Of Ethernet	6
1.3.2	Media Access Control	11
1.3.3	Ethernet Packet Structure	12
1.4	Out Line Of The Rest Of The Thesis	14
CHAPTER 2	MAU AND TRANSCEIVER FUNCTION	15
2.1	MAU	15
2.2	Transceivers	17
2.2.1	Description	17
2.2.2	Operation	19
CHAPTER 3	REPEATER	21
3.1	Introduction	21
3.2	Signal Regeneration	23
3.3	Collision Detection And Jam Generation	25
3.4	Design Considerations	27
3.4.1	Signal Amplification Retiming And Data Repeat	30
3.4.2	Preamble Bit Insertion	33
3.4.3	Collision/Jam Signal Generation	36
3.4.4	Fragment Extension	38

CHAPTER 4	HARDWARE DETAILS	39
4.1	Details Of Circuits	39
4.1.1	System Clock Generation.....	39
4.1.2	Input Block	42
4.1.3	Memory Block	42
4.1.4	Control Block	45
4.1.5	Preamble And Jam Generation	47
4.1.5	Output Block	47
4.2	Complete Circuit And Timing Diagrams	50
CHAPTER 5	PERFORMANCE AND CONCLUSION	56
5.1	Fabrication.....	56
5.2	The Test Set-up And The Performance Check	56
5.3	Performance On Network	58
5.4	Specifications of Repeater	61
5.5	Conclusion	61
REFERENCES		63
APPENDIX	SGS Thomson Microelectronics Data Sheet	
	For MK 45H02-N 35 FIFO	

ABSTRACT

A Local Area Network consists of a variety of sub system such as the physical media, host computer interfaces for the LAN, a medium access control mechanism and others. Whenever a LAN such as Ethernet needs to be extended beyond the limits of a physical medium such as a coaxial cable, due to signal attenuation and distortion, the job is done by sub systems such as Repeaters, Bridges or Routers.

The repeater is a physical layer device which amplifies and retimes the signal from one side of the network to another within the acceptable delay. In this work, the design and successful implementation of a Repeater conforming to IEEE 802.3 Ethernet standards is described. The actual implementation details are described after a presentation of an overview of the Ethernet standard. The hardware has been fabricated in wirewrap form using fast TTL MSI ICs and FIFOs. The performance measurements of the Repeater were carried out on a LAN test-bed. The results show that the Repeater has almost no error and conforms to the standards.

Chapter 1

INTRODUCTION

1.1 COMPUTER NETWORKS

When a large number of identical or different computers are interconnected and communicate information with each other, it is known as "COMPUTER NETWORK". Logically a network can be in one room or in one building or in one institution or in one city or in one country or around the globe itself. Depending upon the need for the network it is partitioned in different terms such as

1. Local area network LAN This spans a few kms
2. Metropoliton area network MAN This spans 10s of kms
3. Wide area network WAN This spans across a geographical region

Typical services rendered by a computer network are

1. Remote log-in
2. File transfer
3. Electronic mail
4. Directory services

Some networks are also used for real time distributed applications such as industrial process control and defence application.

In a LAN, it is not always possible to accomodate all systems in one segment. One way to increase the span is to use more than one segment and interconnect them using REPEATERS, BRIDGES or ROUTERS.

A repeater is a physical layer device. It receives, amplifies, and retransmits signals in one or both directions as needed. Thereby it compensates for distortion, cable losses and timing jitters. A bidirectional repeater connecting two ethernet segments is shown in fig. 1.1.

A bridge is a type of product that links different local area networks enabling users on the one network to use all the resources available on the other.

A router is a machine in a large network that reads the destination of a message and selects the best route.

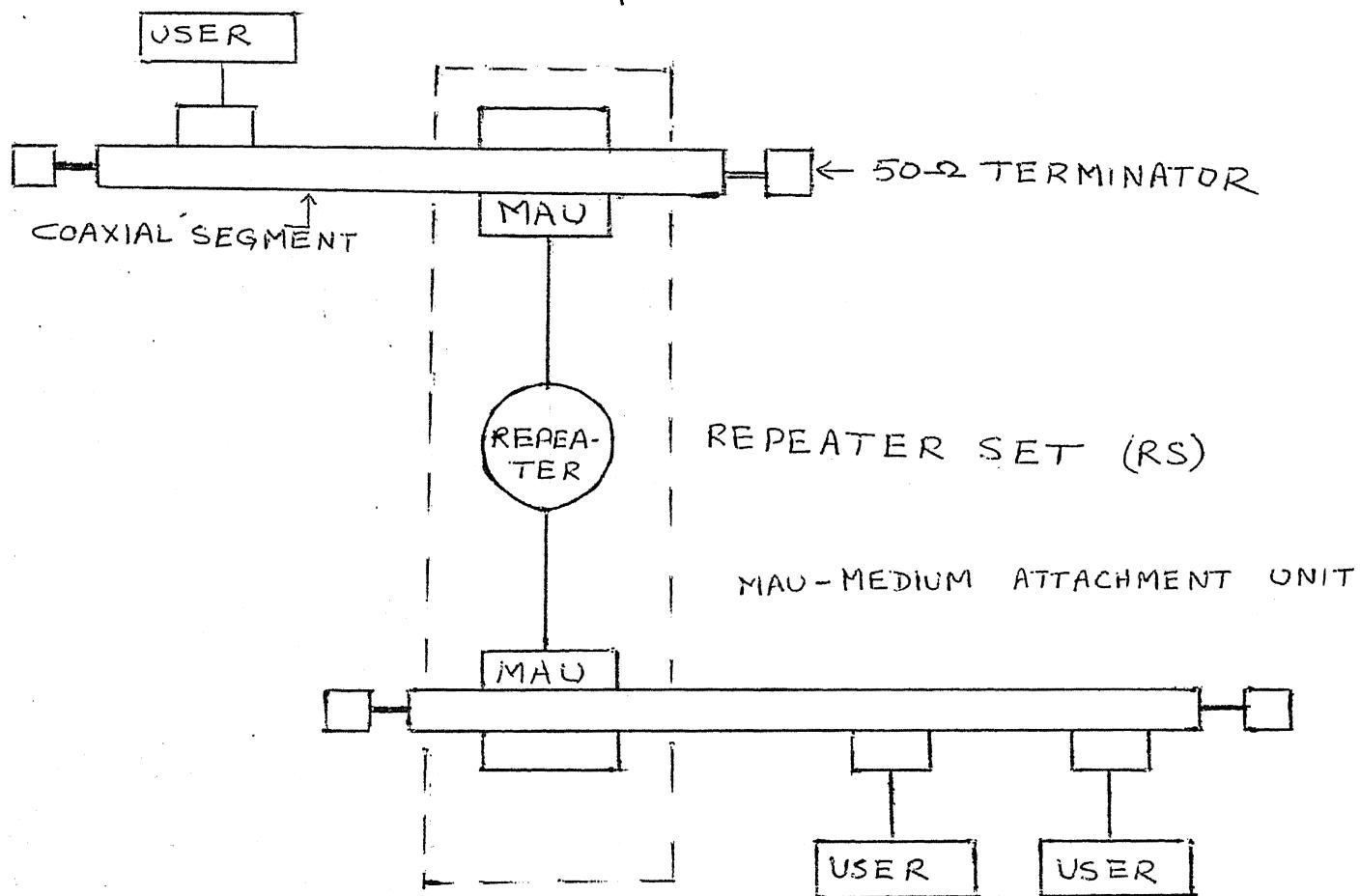
An introduction to computer network can be found in [1]. In this work, the design and implementation of a repeater conforming to IEEE 802.3 Ethernet standards is described.

1.2 STANDARDS FOR NETWORKS

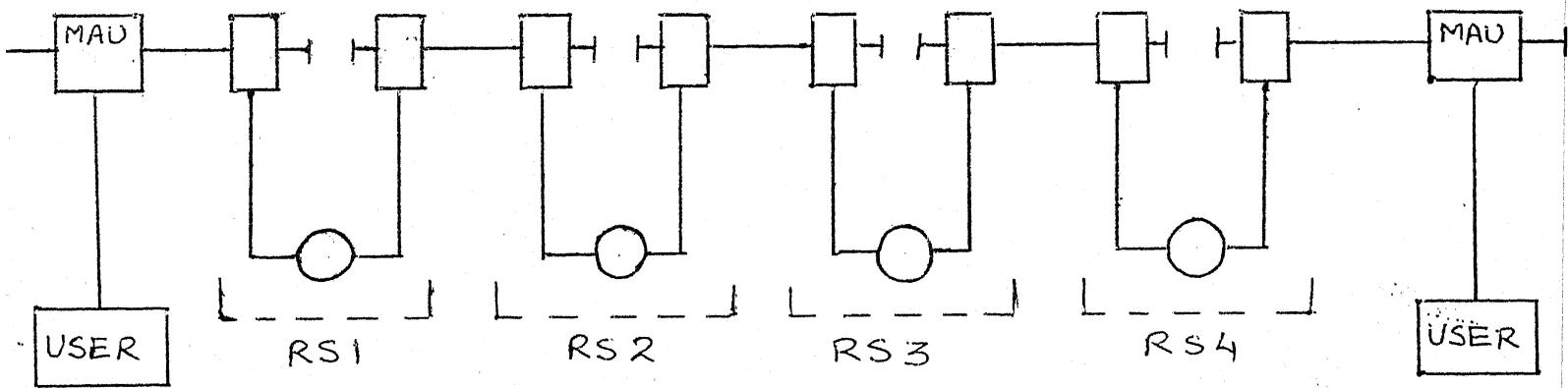
The INTERNATIONAL STANDARD ORGANISATION [ISO] developed an OSI [OPEN SYSTEM INTERCONNECTION] reference model as a frame work to describe the functional architecture of networks.

1.2.1 Open System Interconnection (OSI)

The OSI reference model consists of seven layers as follows:



MINIMUM SYSTEM CONFIGURATION USING REPEATER SET



MAXIMUM TRANSMISSION PATH

FIG. 1.1

1.2.1.1 PHYSICAL LAYER

The physical layer describes the physical media over which the bit stream is transmitted. Such specifics as type of cable (Coaxial, twisted pair etc) signal levels, bit rate, connectors to be used etc are described in the physical layer specification. In short, it describes the actual physical media over which the bit stream is transmitted and the method of transmissions.

1.2.1.2 DATA LINK LAYER

The data link layer describes the rules for transmitting on the physical media. Such items as the format of the information (or frame) and procedures for obtaining control of the physical media (referred to as the media access methods) transmitting the frame and releasing the physical media, error detection, ARQ and frame sequencing are described in the data link layer.

1.2.1.3 NETWORK LAYER

The network layer governs the switching and routing of information between and inside the networks. Because all station to station communication within a single local area network is point to point, the network layer is not necessary for a single LAN system.

1.2.1.4 TRANSPORT LAYER

The transport layer assures end to end integrity and provides for the required quality of service for exchanged information. End to end acknowledgements of successful message receptions and different connection type are performed by the transport service, for example.

1.2.1.5 SESSION LAYER

The session layer manages the requesting and deleting of virtual circuit connection services provided by the transport layer. This is also responsible for the mapping of logical names to network addresses.

1.2.1.6 PRESENTATION LAYER

The presentation layer provides for any necessary translation, format conversion or code conversion to put the information into a recognisable form.

1.2.1.7 APPLICATION LAYER

The application layer directly serves the communicating end user application process by providing the distributed information service appropriate to the application and its management. Network services such as file server, electronic mail or virtual terminal protocols are provided by the application layer.

By implementing a particular physical and data link specification, equipments from multiple vendors can be physically and electrically connected. The physical and data link layer of the OSI model assure inter-connectivity. The remaining five layers of the OSI model assure inter operation among the interconnected stations in an open network.

1.2.2 IEEE 802 Series

IEEE has issued a series of network standards. These standards specify several popular networks upto the data link layer. The different IEEE 802 standards which include CSMA/CD, Token bus, Token ring etc, are as follows:

- IEEE 802.1 Relationship among the 802 series standards and the OSI reference model
- IEEE 802.2 Logical Link Control Standard
- IEEE 802.3 CSMA/CD based LAN (ETHERNET)
- IEEE 802.4 Token Bus Network
- IEEE 802.5 Token Ring Network
- IEEE 802.6 Dual Queue Dual Bus Broadband Fibre Network (DQDB)
- IEEE 802.7 Fibre Distributed Data Interface Broadband Network (FDDI)

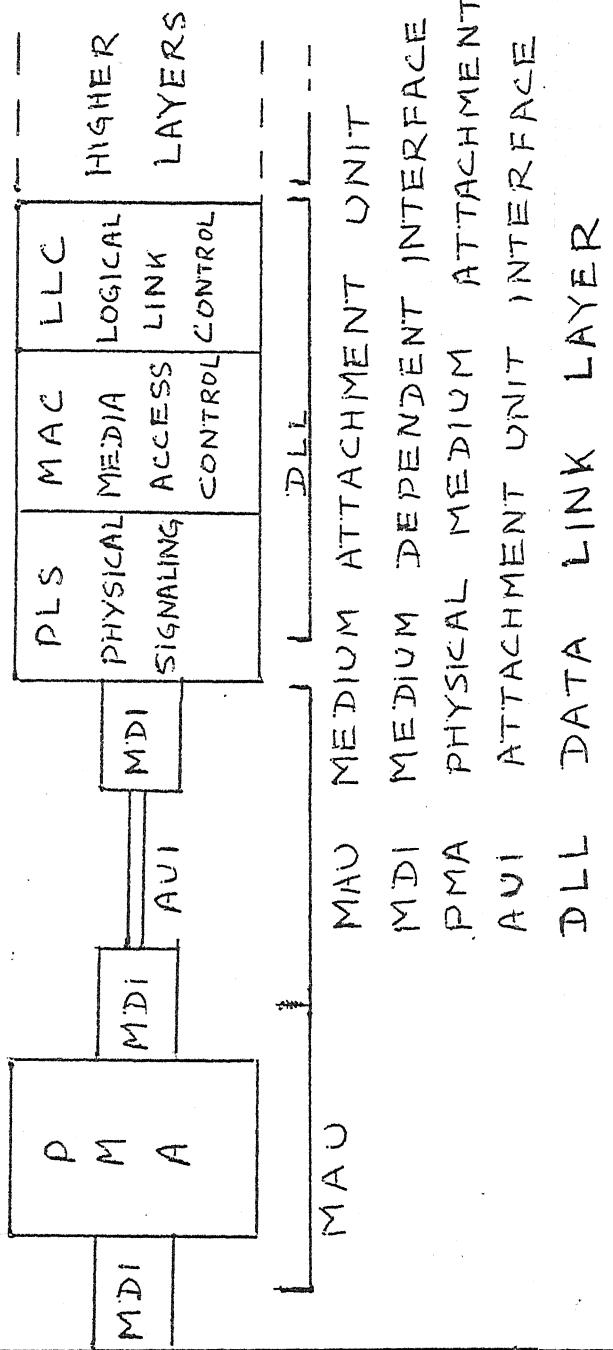
Only the IEEE 802.3, commonly called as Ethernet will be referred to in the rest of this work. The Ethernet is a coaxial cable based Bus network. It carries typically 10 MBPS of data in packetised form from one user at a time using a CSMA/CD/BB protocol.

1.3 IEEE 802.3 STANDARD

1.3.1 *Physical Layer of Ethernet*

This IEEE Standard is organised along architectural lines, emphasizing the large scale separation of the system into two parts: the Media Access Control (MAC) sublayer of the Data Link Layer (DLL), and the Physical Layer. These layers are intended to correspond closely to the lowest layers of the ISO model for Open System Interconnection (OSI) as shown in fig 1.2. The Logic Link Control (LLC) sublayer and MAC sublayer together encompass the functions intended for the Data Link Layer (DLL) as defined in [3].

← CENTRE CONDUCTOR



COAXIAL →
CABLE

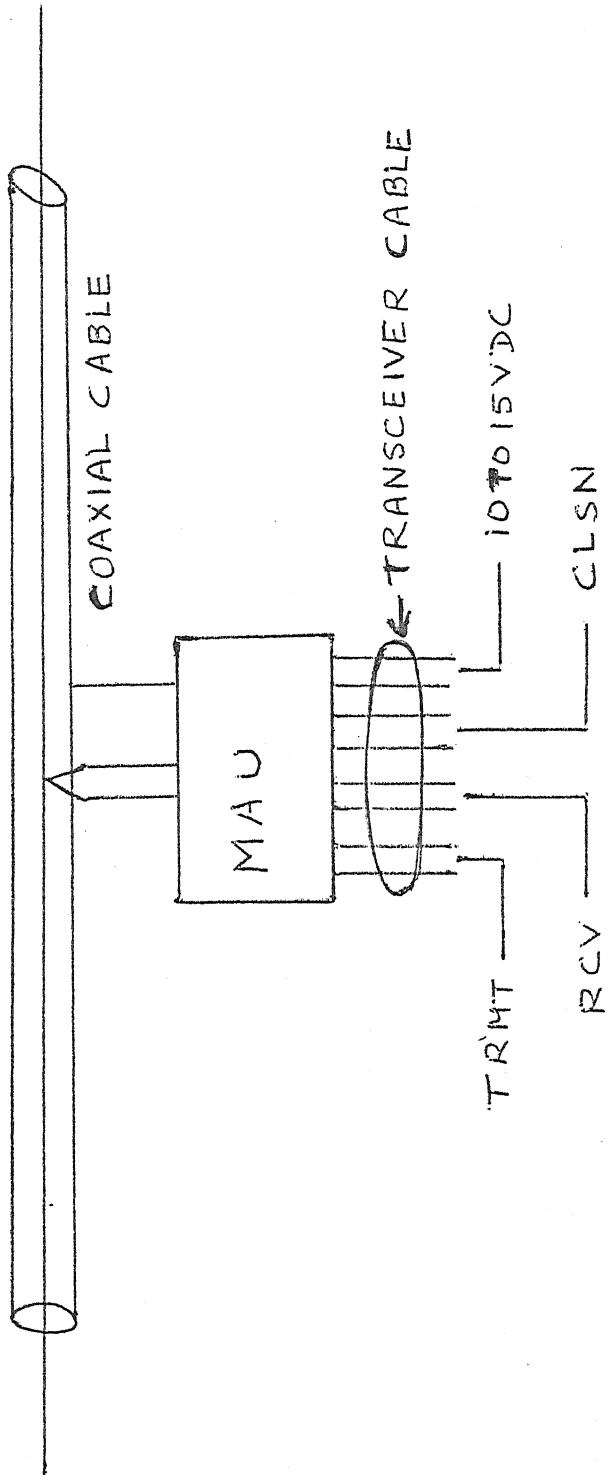
INTERCONNECTION OF PHYSICAL AND DATA LINK LAYER

A small amount of circuitry will exist in the Medium Attachment Unit (MAU) directly adjacent to the coaxial cable, while the majority of the hardware as well as all of the software will be placed within the user node or station. The MDI and AUI are two different interfaces for the requirement of sublayers as shown. The MAU will be discussed in detail in chapter 2.

The interface between the MAC sublayer and the Physical Layer includes signal for framing (carrier sense, transmit initiation) and collision detect, facilities for passing a pair of serial bit streams (transmit, receive) between the two layers and a wait function for timing. Whereas the interface between the MAC and the LLC sublayers includes facilities for transmitting and receiving frames.

The physical connection between the coaxial cable and the user node is through MAU and connecting transceiver cables as shown in fig 1.3. The transceiver cable has a maximum length of 50 meter whereas the coaxial segment spans to a maximum length of 500 meters due to inherent losses in long cables. The coaxial cable (basic Ethernet cable) is tapped in multiples of 5 meters distance along it for the use of user nodes. Standards also specifies the methodology to install large networks spanning upto 2.5 kms using upto 500 meter segment interconnected by Repeaters. For example a large network may have the structure shown in fig 1.4. Repeaters are connected to coaxial cables through MAUs (Medium Attachment Unit). A repeater is a dumb unit which just copies bits blindly without understanding what they are doing. It just forwards bits from one network to another making two networks look logically like one network. Networks are often split in to two pieces due to maximum cable length restriction on the individual pieces which is approximately 500 meters. The standard also provides specifications for input/output behavior of the repeater. More detailed description of the network and the repeater are given in chapter 2 and 3.

PHYSICAL STRUCTURE



LOCAL AREA NETWORKS.

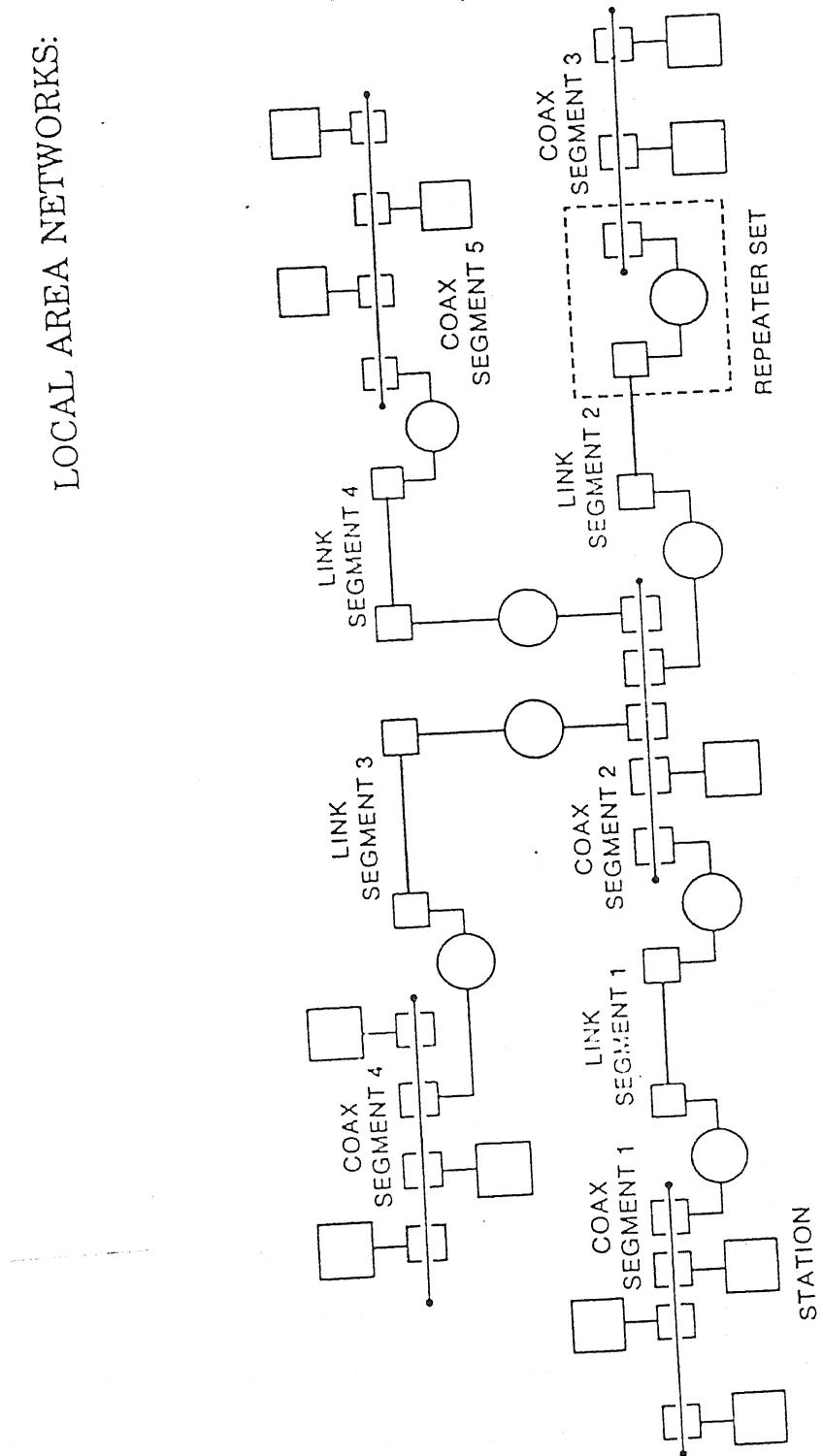


Fig. 1.4
An Example of a Large System with
Maximum Transmission Paths

The signal on the cable is a straight binary transmission (+1.32 v for 1 bit and -0.25 v for a 0 bit) of the Manchester encoded data stream from the DLL. With Manchester encoding, each bit period is divided in two equal intervals. A binary 1 bit is sent by having the voltage be high during the first interval and low in the second one. A binary 0 bit is reverse of it i.e., first low and then high. This scheme ensures that every bit period has a transition in the middle, making it easy for the receiver to synchronise with the sender.

1.3.2 Media Access Control

Sharing of the medium is achieved through Media Access Control MAC [2]. The MAC protocol specifies some systematic methods by which different nodes are allocated access to the communication media. In Ethernet LAN the MAC protocol is the Carrier Sense Multiple Access with Collision Detection and Binary Backoff i.e., CSMA\CD\BB. In this scheme a node listens to the cable or medium to find out whether other nodes are transmitting. This is known as carrier sensing. When a node detects an idle period and it has a packet to send, it initiates packet transmission. Thus any node can have the access to the medium hence called multiple access. While transmitting it also listens to the cable to find out whether a collision of the packet has taken place, if at the same time some other node also transmits on the cable getting the idle state. MAU detects the collision and it sends a collision report to the host to reschedule the transmission. Some algorithm is used for retransmission known as Binary Exponential Backoff. The part of collision detection is done by MAU whereas the part of CSMA and BB is by the LAN controller which is available in the user node i.e., LLC.

1.3.3 Ethernet Packet Structure

The data in the form of one packet is formed as follows:

FIELD	NO. OF BYTES
PREAMBLE BITS	(7)
SFD	(1)
DESTINATION ADDRESS	(6)
SOURCE ADDRESS	(6)
TYPE FIELD	(2)
INFORMATION FIELD	(0-1518)
PAD	(If applicable)
CRC	(4)
EFD	

Fig 1.5

Preamble bits: These are continuous bits of 101010101... for 56 times. This gives the system a notion that some transmission is going to begin on the ETHERNET and after this the ethernet will be busy. This is also required for synchronisation purposes.

SFD: This is 8 bits Start Frame Delimiter constituting 10101011, which makes the controller to understand that now the actual data is pouring in and processing must start as soon as the last two consecutive ones(is) is received.

Destination Address (DA): It gives the address of the station for which the information is intended to. As the transmission is heard by all the user on the network, the destination address only will actuate the specific user to receive it. If the D A is all '1' then it is called a broadcast packet and all users will accept

the information. If it is for a group of users then named as multicast. This has a length of 48 bits.

Source Address: It gives the address of the sender's computer. This also has a length of 48 bits.

Type Field: It has a length of 16 bits and gives the type of the message such as IP, ARP, SNMP etc

Information Field: It gives the full contents to be sent. This varies from 46 bytes to 1500 bytes. Depending upon this field the size of the packet is measured.

PAD: This field is a sequence of octets which are added at the end of information field to increase the packet size to a minimum of 64 bytes if the information size is small. This works like a pad.

CRC: It is known as check sum or cyclic redundancy check. It is a 32 bits hash code of data and used as parity checker for the full text of information.

EFD: It is End Frame Delimiter giving the idea of end of frame indicated by the lack of signal after transmitting the last bit of CRC.

The minimum and maximum frame size limits of 64 bytes and 1518 bytes respectively refer to the portion of the frame from Destination address to CRC field, inclusive.

The basic ethernet is called as thicknet or 10 base 5. This stands for a LAN operating at 10 MBPS and spanning 500 meters without repeaters. There are two more variations of Ethernet described in the supplement to the standards. One is 10 base 2 operating at 10 MBPS and spans to 200 meters. The other one is 10 base T operating at 10 MBPS using twisted pair cables.

1.4 OUTLINE OF THE REST OF THE THESIS

Chapter 2 begins with the media and transceiver units as well as transceiver cables. It also deals with collision detection part in it.

Chapter 3 deals with the design considerations and the required components towards the implementation of repeater. It also conforms to the IEEE 802.3 standards requirements.

Chapter 4 stretches the design to hardware details and the explanations of all blocks including the timing diagrams.

Chapter 5 gives the test results and the performance of the fabricated repeater as well as the behavior on the main network. It also gives the concluding part and the ideas of futuristic developments concerning the repeater.

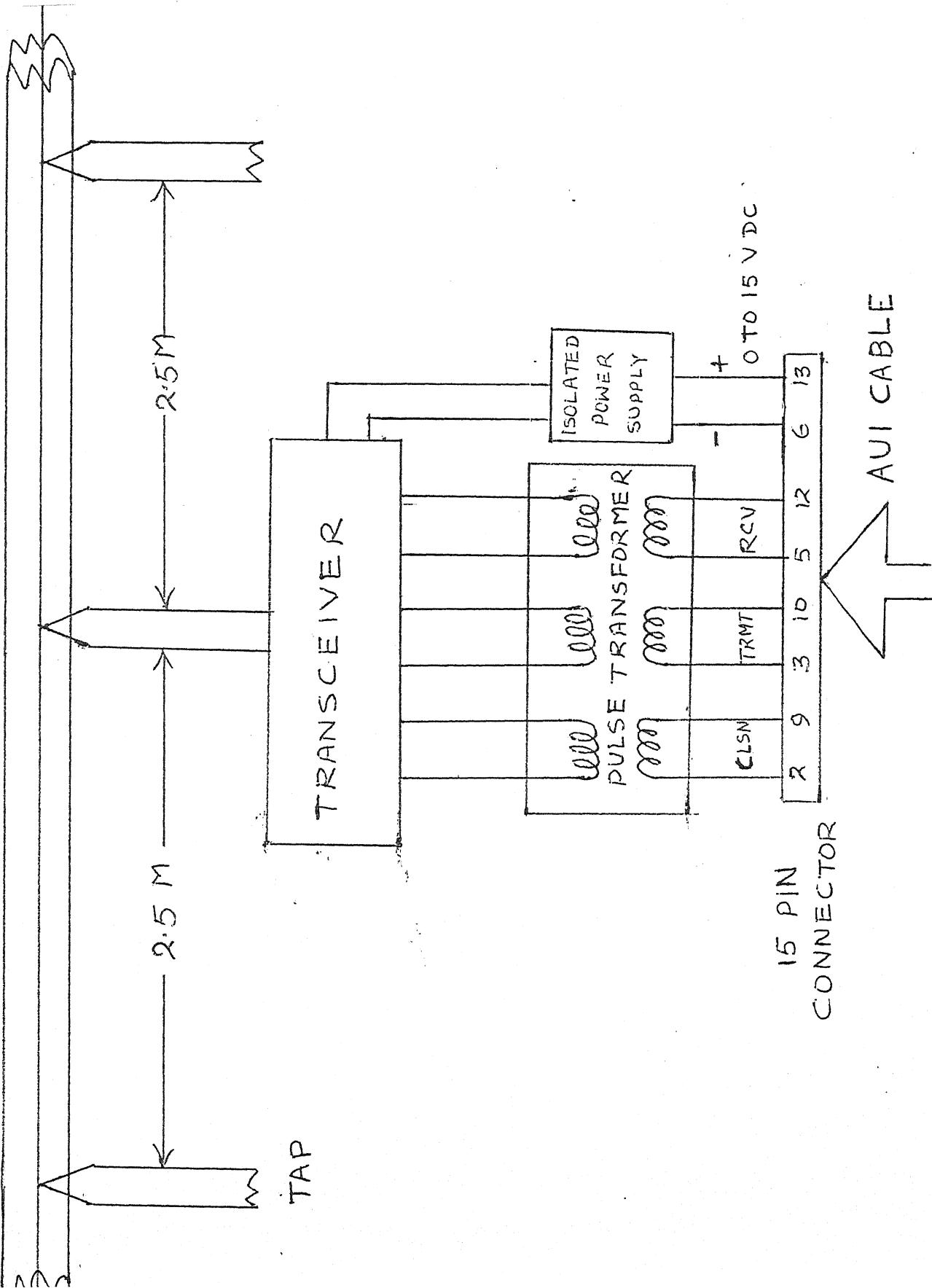
Chapter 2

MAU AND TRANSCEIVER FUNCTIONS

2.1 MAU (MEDIUM ATTACHMENT UNIT)

As shown in the fig 1.1 the connection of a host to the Ethernet is made through Medium Attachment Unit. In the network the packets travels on the coaxial cable. The user computer taps the data from the cable with the help of transceivers at a gap of minimum 2.5 meters along the cable and four pair transceiver cables. The transceiver taps the data from the cable and makes it to go to the RCV pair of transceiver cable which feeds to the user station. When the user tries to send the data it sends on to the TRMT pair of transceiver cable which then again passes on through transceiver unit to the coaxial cable. In case of collision the collision detect signal is passed to the user node on the CLSN pair of the cable. Transceiver units clamp securely to the coaxial cable and the transceiver cable connects the user computer to it. The transceiver cable has a maximum length of 50 meters. The whole configuration is termed as Medium Attachment Unit (MAU) and has been shown in fig.2.1. The transceiver unit will be discussed in section 2.2 of this chapter.

The output of transceiver unit is connected to transceiver cable through pulse transformers. The transformer provides the isolation required between the



transceiver cable and the coaxial cable. +12 volt dc is supplied to the Isolation Power Supply for 5 volt and 15 volt supplies required by the MAU.

The 4 pair cable serves the following purposes:

1. TRMT For transmission
2. RCV For reception
3. CLSN For collision
4. Power For +12 volt dc supply

The MAU has the following functions:

1. It supports message traffic at 10 MBPS.
2. It provides a length of 50 meter towards repeater from coaxial cable.
3. It supports in handling collision detection.
4. It supports in making the right path for transmission and reception.
5. It provides a self test for collision detection circuitry by means of SQE test.
6. It permits the data terminal equipment to test the medium.
7. It has the ability to automatically interrupt the transmit function and inhibit an abnormally long output data stream known as jabber function.

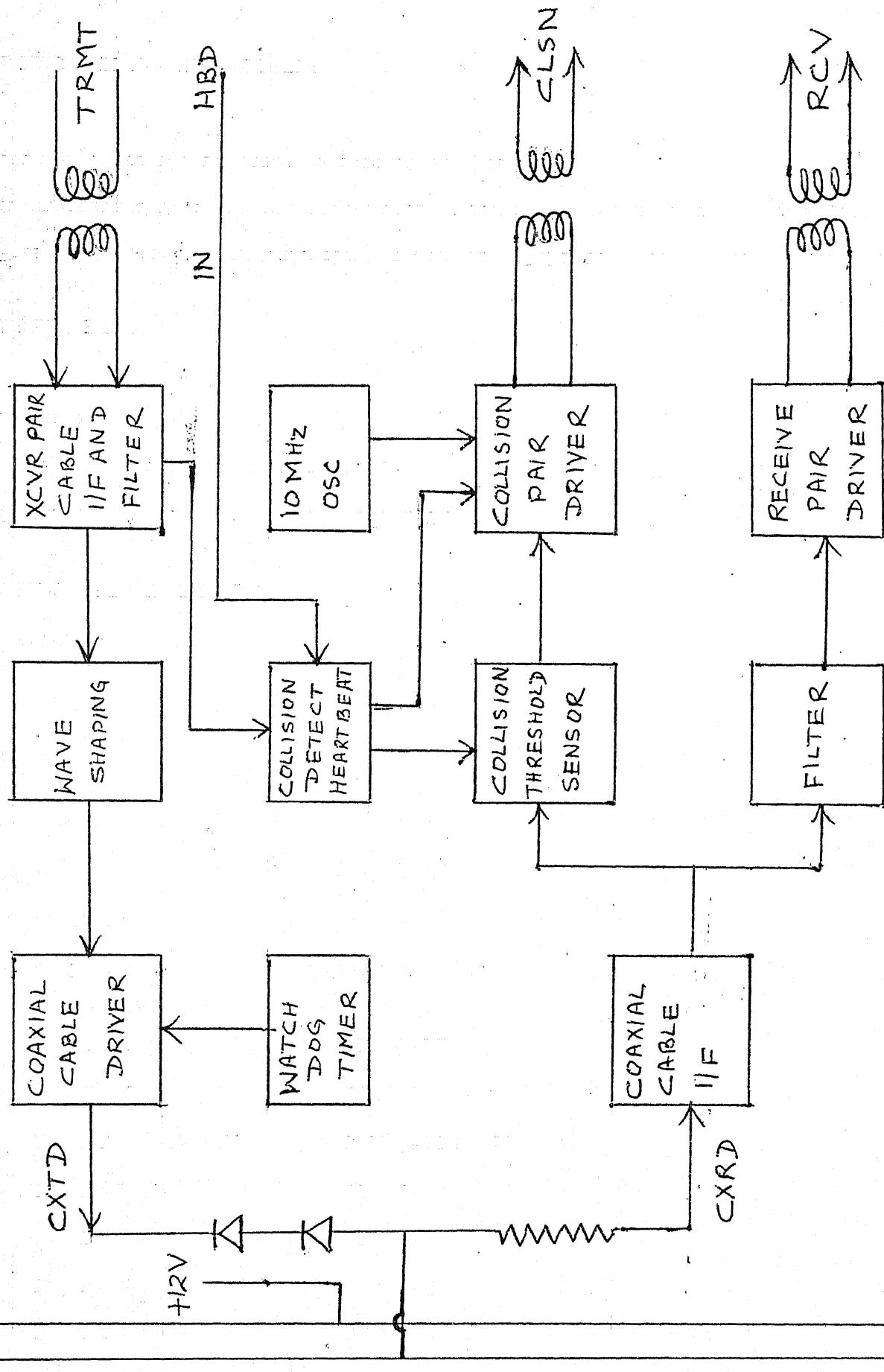
2.2 TRANSCEIVERS

2.2.1 Description

The transceiver unit is an integral part of MAU as well as of Repeater. This forwards the Manchester coded data to the station or to the coaxial cable. The diagram of the internal blocks of the transceiver unit is shown in fig. 2.2. The

TRANSCOMMUNICATOR UNIT

FIG. 2.2



CXTD is the signal transmitted from the station to the cable and CXRD is the received data from the cable to be forwarded to the user station connected to it. This has the following portions of operations:

1. Receives signal from the station and sends out to the medium.
2. Receives signal from the medium and sends out to the station.
3. Detects collision and warns the station.
4. Protects the medium from an extra ordinary long message known as Jabber Function.

2.2.2 Operation

2.2.1.1 TRANSMISSION

When the manchester encoded data reaches on to TRMT pair from a user computer it goes out to the CXTD of the transceiver after the noise filtering and proper waveshape formation. Due to the proper biasing at coaxial cable end the data is passed over to cable and at the same time is received back on the CXRD. So the data being transmitted is received back to have a sense of check. In case of heart beat check the system works in a loop back mode for testing.

2.2.1.2 RECEPTION

The data which is flowing in manchester encoded form on the coaxial cable is received on CXRD as well as if transmitted from the CXTD. The received data is passed through filter and receive pair driver to be output through RCV pair on to the RCV pair of transceiver cable.

2.2.1.3 COLLISION DETECTION

If two stations or users have transmitted data on coaxial cable simultaneously, then both will reach on CXRD and the increase in current level will be sensed in the collision threshold sensor. This will cause a 10 MHz oscillator output on CLSN pair of transceiver cable causing a collision detect signal. It is also known as "JAM" signal as it jams the network for a while and all user stops transmission on the media and waits for a random period of time before retrying.

Similarly if a data has been transmitted from CXTD on to the coaxial cable, then it is also received back on CXRD as feed back. So if another station starts transmitting at the same time it will also reach on the CXRD and again collision threshold sensor will sense an increase in current level causing a collision detect signal output on CLSN pair of transceiver cable. There is a provision known as Signal Quality Error (SQE) or Heart Beat Disable (HBD) test in the transceiver that if HBD input is strapped low, then the self test feature of the transceiver is enabled. If it is enabled then at the end of each packet transmission, a local collision test signal of 10 MHz is generated for 0.5 to 1.5 μ sec period i.e. 5 to 15 pulses of 10 MHz clock. This tests the health of the collision detection circuitry of the transceiver unit. If HBD input is pulled high then this test is disabled. This HBD test signal also goes to the user stations on the CLSN pair of transceiver cable. This is usually discarded by the LAN controller as a test signal.

2.2.1.4 JABBER FUNCTION

The watch dog timer start operating as soon as the CXTD becomes active. So if the packet is lasting for more than 25 ms the MAU stops the transmission to the media. Generally the maximum duration of one packet is approximately 1.25 ms.

Chapter 3

REPEATER

3.1 INTRODUCTION

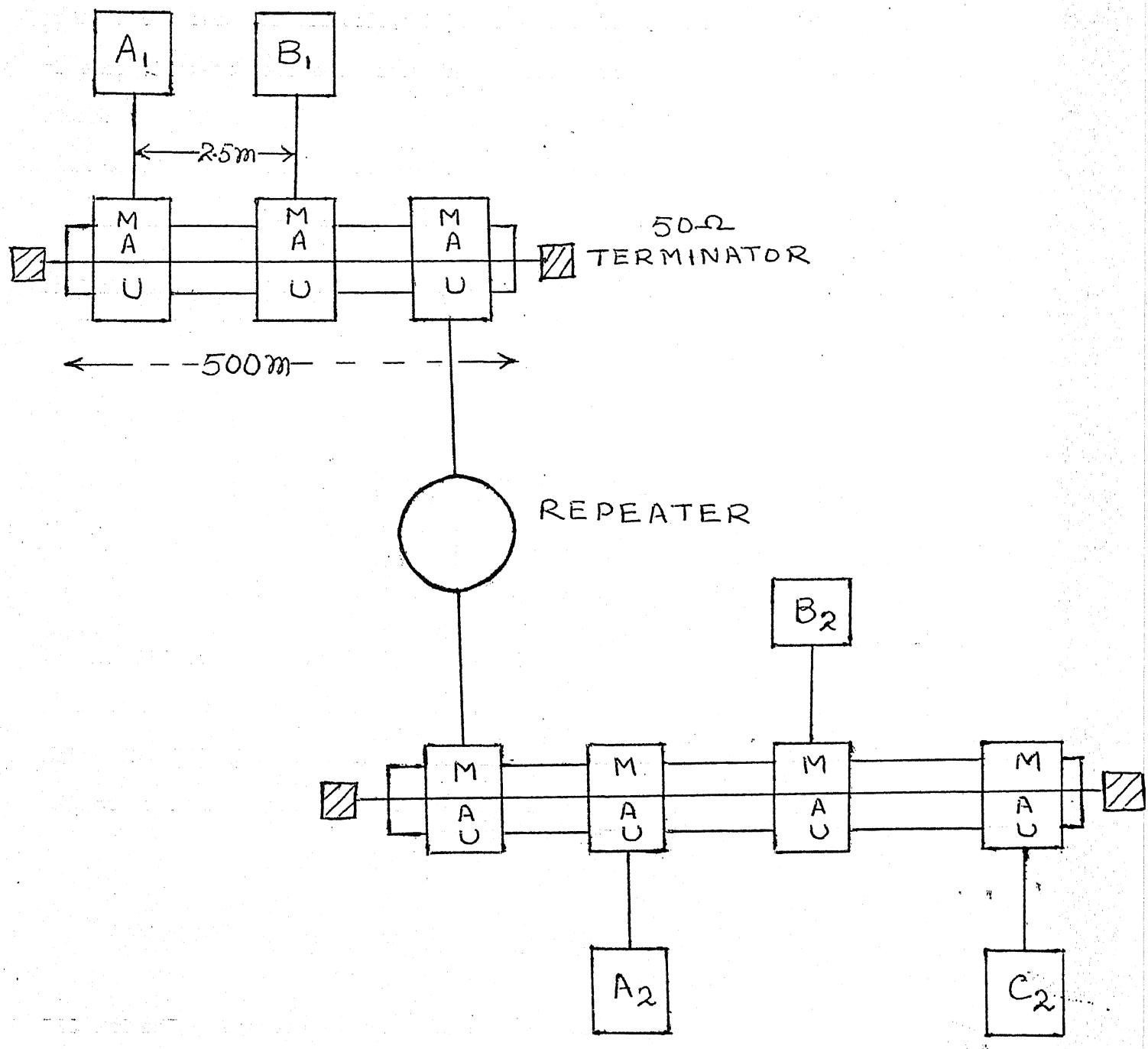
The repeater unit is used to extend the network length and topology. It interconnects two segments of Ethernet at the Physical Layer level. Several Repeaters can connect several Ethernets to make a large network, but a maximum span of 2.5 kms can only be achieved between two communicating nodes. The end to end connection of the segments can be configured as shown in fig 3.1.

The functions of the repeater can be appreciated as follows:

1. That whenever any node A1 transmits a packet on one segment, the repeater picks it up and retransmits to another segment with a minimal delay.
2. That if two nodes on two different segments transmit almost at the same instant, the collision occurs at the repeater. Then as per the CSMA\CD protocol the repeater must report this as a collision to both the segments.

This chapter describes the various specifications and design considerations of an Ethernet Repeater. The properties of a repeater are as follows:

1. It supports message traffic at 10 MBPS.
2. It provides for driving upto 500 meters of coaxial cable.
3. This should not incur a delay of more than 7.5 bit time i.e. 0.75 μ sec in taking the signal from one end of repeater to another.



END TO END CONNECTION OF TWO SEGMENTS

FIG 3.1

To achieve this the repeater must support various functional requirements as follows:

3.2 *SIGNAL REGENERATION*

3.2.1 *Signal Amplification*

The repeater set shall ensure that the amplitude characteristics of the signals at output of the repeater are within the tolerance of the specification for medium attachment unit output. Therefore loss of signal due to cable loss and noise pickup is restored at the output of the repeater.

3.2.2 *Signal Symmetry*

The repeater shall ensure that the symmetry characteristic of the signals at the MAU outputs of the repeater set are within the tolerance of the specification for MAU output. Therefore any loss of symmetry due to MAUs and cable distortion is regained at the output of the repeater.

3.2.3 *Signal Retiming*

The repeater unit shall ensure that the encoded data output from the repeater unit is within the jitter tolerance of a transmitting DTE(Data terminal equipment). Therefore jitter can not accumulate over multiple segments.

3.2.4 Carrier Sense and Data Repeat

The repeater set shall implement the carrier sense function for both the cables to which it is connected. Upon detection of carrier from one segment, the repeater set shall repeat all received signals from that segment on to the other segment

3.2.5 Preamble Insertion

The repeater unit shall output atleast 56 bits of preamble followed by the start frame delimiter. As due to the loss of first few bits in each repeater may cause a total loss of preamble bits after passing through many repeaters. So preamble bits are made up in each repeaters.

3.2.6 Data Propagation Delays

The data propagation delay for a repeater unit is complicated by the bit insertion requirement. The data propagation delay is specified in terms of the first bit in to the first bit out and the last bit in to the last bit out, which are 7.5 bit times and 9 bit times respectively.

3.2.7 Fragment Extension

If the signal being repeated is less than 96 bits in length including preamble, the repeater shall extend the signal with artificial data (generated by the repeater unit) so that the total number of bits output from the repeater unit shall equal 96. The data sent to perform the extension may have any value except the occurrence of the SFD. Our implemented repeater sends out a sequence of 101010... as artificial data.

3.2.8 Collision Related Functions

This is one of the most basic function of the Ethernet repeater to ensure reliable operation of the CSMA\CD protocol. There are many conditions associated with this. Their functions are described in next section.

The entire description of collision detection and jam generation is available in the state diagram shown in fig 3.2. The collision is detected in MAU and MAU sends a collision signal to the repeater. In an ideal case the network is idle and the packet of data coming from side 1 is repeated to side 2 and at the end of packet transfer it goes to idle state. If the packet is of less than 96 bits time duration then a sequence of some bits are sent to other side for 96 times and at the end of it, it comes to the idle state. If a collision is sensed at one side then jam signal is sent to both the sides for 96 bit time period. After the jam signal it again goes to idle state.

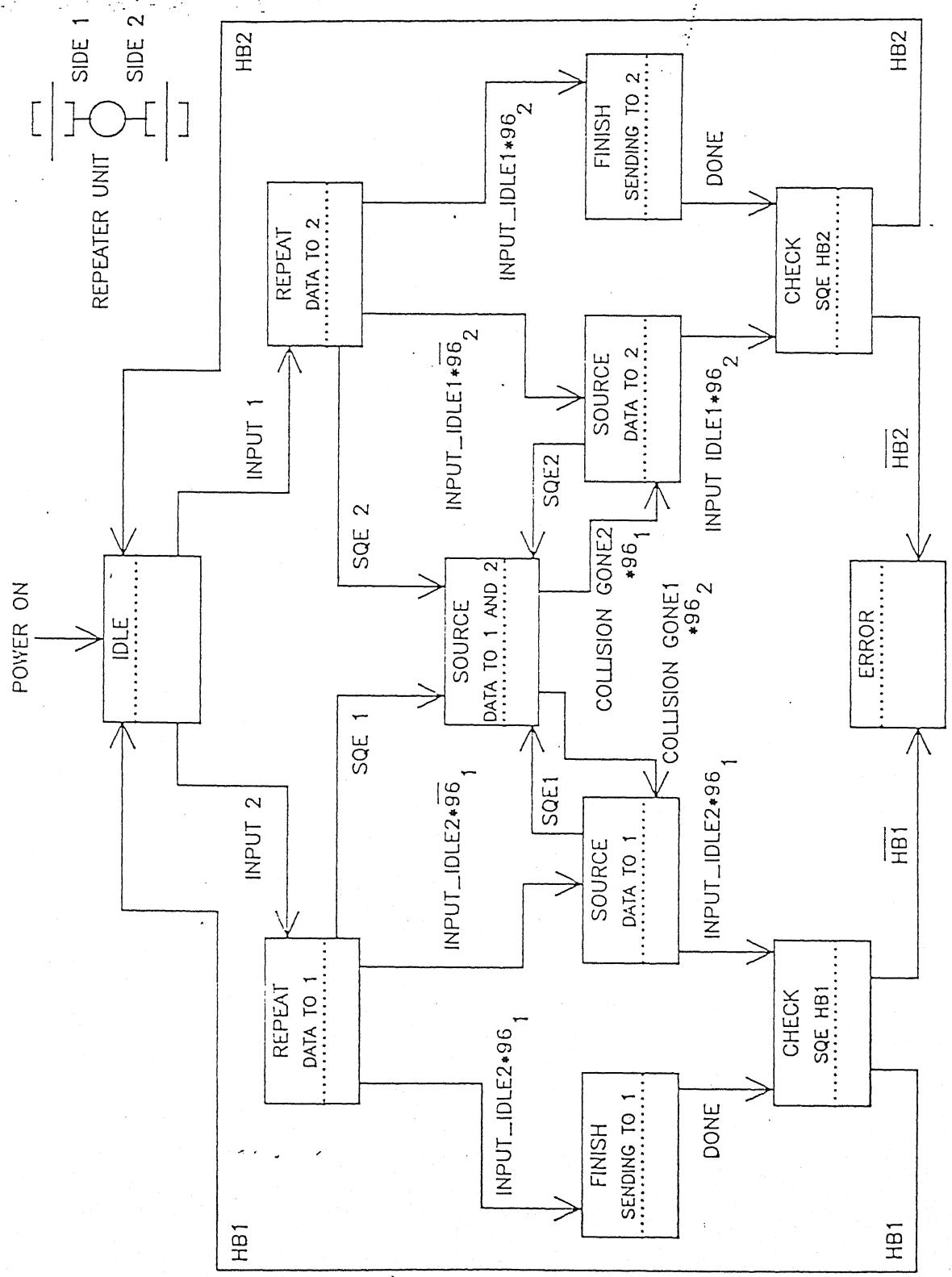
3.3 COLLISION DETECTION AND JAM GENERATION

3.3.1 Collision Presence

The repeater set shall implement the collision presence function for both segments to which it is connected. So whenever a collision signal is received at one side it gives a collision detect signal indicating the presence of collision.

3.3.2 Jam Generation

If collision is detected on the side to which the repeater set is transmitting, the repeater set shall transmit a jam signal to both of the segments to which it is



connected. The jam signal shall be transmitted in accordance with the repeater unit state diagram in fig 3.2.

3.3.3 Collision - Jam Propagation Delays

The collision propagation delay is the period of time between the assertion of the collision detect signal and the first bit of jam output which is ≤ 6.5 bit times.

3.4 DESIGN CONSIDERATIONS

The design of the repeater was considered on the following lines:

1. As soon as data is received at the input it is repeated to other side for onward transmission as soon as possible.
2. In case a packet of size less than 96 bits is received then a sequence of 101010... is added to it to make it 96 bit packet and transmitted.
3. If a collision signal is received at input then the repeater should send some information to both sides of the network which has no validity known as JAM signal and the network is kept busy. In this repeater a sequence of 101010... is sent as jam signal for 96 bit time.
4. There is a chance of a data to be received at one end of repeater when the other end is also busy in getting data and repeating it. This should be taken as a collision and both sides should again get some jam signal.

The whole thing is shown in the flow chart as shown in fig. 3.3

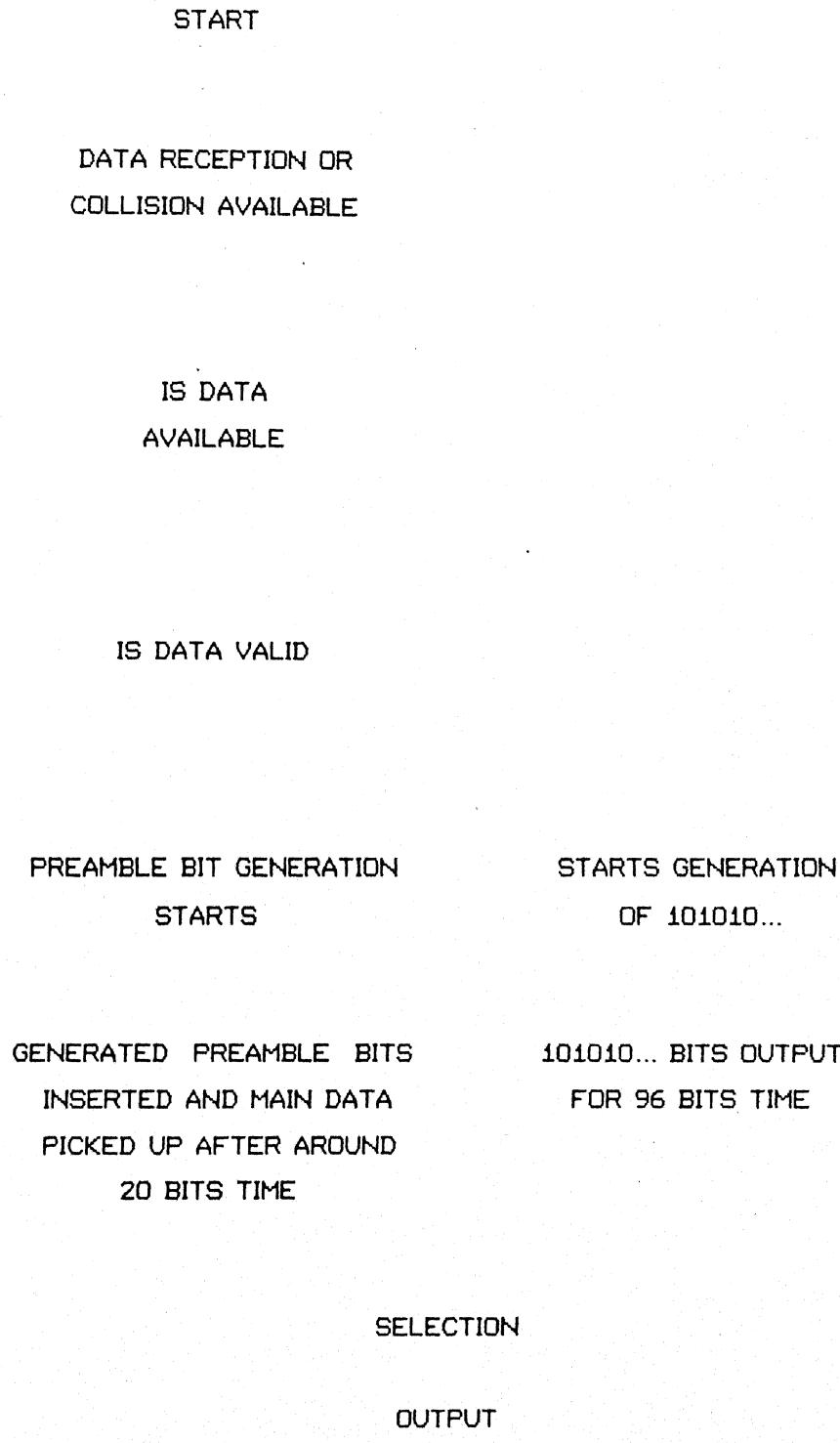


FIG. 3.3

5. The repeater should not be connected to a transceiver which has the SQE parameter enabled. Due to enabled SQE the repeater will get a local collision test signal for 0.5 μ sec to 1.5 μ sec causing a generation of collision signal through the repeater to both ends. So SQE of the transceiver must be disabled if a repeater is connected to the transceiver.

An Overview: The first and foremost criterion in the design was to convert the manchester encoded data into NRZ form for proper handling at TTL level. Which goes through the noise filtration too and also gets amplified. The correct integrated chip for this was selected as 82C501 ETHERNET SERIAL INTERFACE (ESI) Chip [5]. Which has the following important functions:

1. Conforms to IEEE 802.3 10 BASE 5 Standards.
2. 10 MBPS operation.
3. Manchester encoding/decoding and noise filtering.
4. 10 MHz clock generator.
5. It replaces several MSI components.
6. As soon as data is received to this chip it gives a carrier sense signal. Which can be used to trigger different control circuits in the repeater unit.
7. On reception of 10 MHz clock at CLSN pair it gives a collision detect signal.

On the basis of this ESI chip the further development was taken up in the form of the following blocks:

1. Signal amplification, Retiming and Data repeat.
2. Preamble insertion.
3. Collision and jam signal generation.
4. Fragment extension

3.4.1 *Signal Amplification Retiming and Data Repeat*

3.4.1.1 BEHAVIOR OF E S I

Output of E S I chip which is in N R Z form after the noise filtration has to be decoded in Manchester form to travel on the next leg of coaxial cable. So the other side of the repeater should also have an E S I chip which will do this job. For this the NRZ formed data must be in synchronisation with the TXC clock of the ESI chip of the other end.

When the data is received at the RCV pair of the ESI chip it gives a carrier sense signal by active low CRS. Then it takes around 1400 n sec time to give out RXC clock recovered from the received data and data out RXD which is in NRZ form. The RXC and RXD are in synchronisation. It is shown in fig 3.4. The RXD is stable for minimum of 45 n sec at the negative going edge of RXC. As from the last paragraph the data out should be stable and in synchronisation with TXC of ESI at the other end, but the RXC and TXC are not in synchronisation. So it is not possible to directly use the same data RXD with TXC. So some method was thought of that if received data is stored in a place with clock RXC as write pulse which can be read by any other clock ie, TXC as read pulse which is not in synchronisation with RXC. For this different type of memory chips were tried out but the problem of addressing was faced. Even normal FIFO chips did not work out due to two different addressing device requirement.

3.4.1.2 SELECTION OF FIFO

Addressing techniques for reading and writing the same memory separately caused lot of delays and circuit also became cumbersome consisting of number of

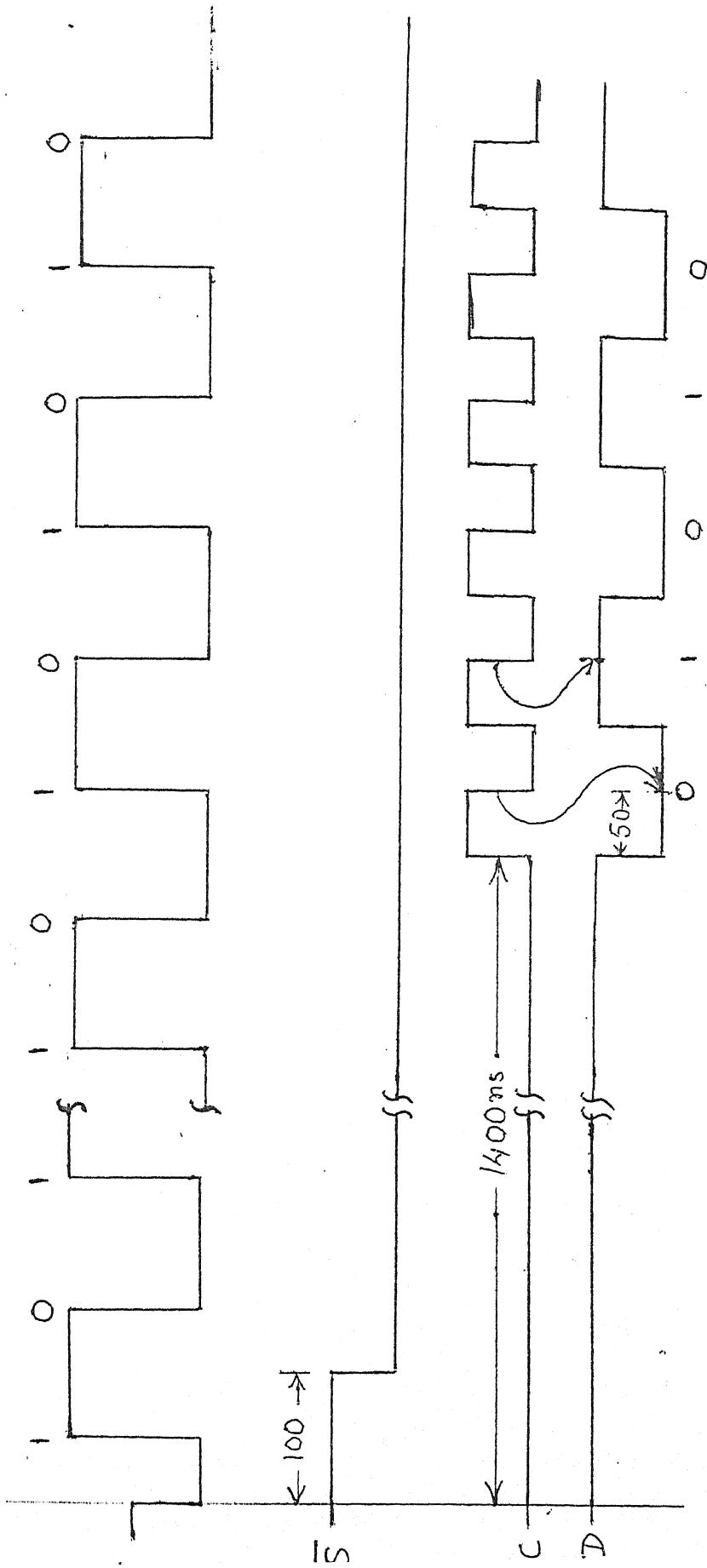


FIGURE 3.4

components. To avoid this MK45H02 CHMOS FIFO of Thompson CSF was used. This FIFO is 1 K bit depth and 9 bit wide for parallel data operation but as repeater requirement is a serial data in/out so only one bit of it was used. This FIFO has the asynchronous and simultaneous write and read operation. The latency of retrieval of data is approximately one write cycle. This chip can go for 28 MHz operation. Though this chip can be cascaded for increasing depth and width but only one chip served the purpose. As the data is simultaneously written and read it can keep on writing and reading by going to zeroeth location after it has reached to the end of depth every time. At each 1024 clock cycles it starts from zeroeth location.

If data is not read at all then the writing stops and there is no over writing in the memory locations. Similarly if the latency of reading and writing is less than one clock cycle then reading stops to give a margin between reading and writing locations causing a random data insertion for one clock pulse.

3.4.1.3 OUTPUT PHILOSOPHY

The data read from FIFO is then passed through shift register which then taken out to a MUX. The idea of shift register is two folds:

1. Encounter the effect of tristateness of FIFO output.
2. To get in phase and out of phase data out of FIFO to be compared with generated preamble bits.

The correctly selected data is made to follow the preamble bits after 20 cycles of activity at the input of repeater.

The data which is now read as well as shifted with the help of TXC clock is in synchronisation with it. So to get the correct synchronisation of data out and

TXC clock, the data out was passed through a delay circuit to get a delay of about 25 n sec. The delay circuit is shown in fig. 3.5.

3.4.2 *Preamble Bit Insertion*

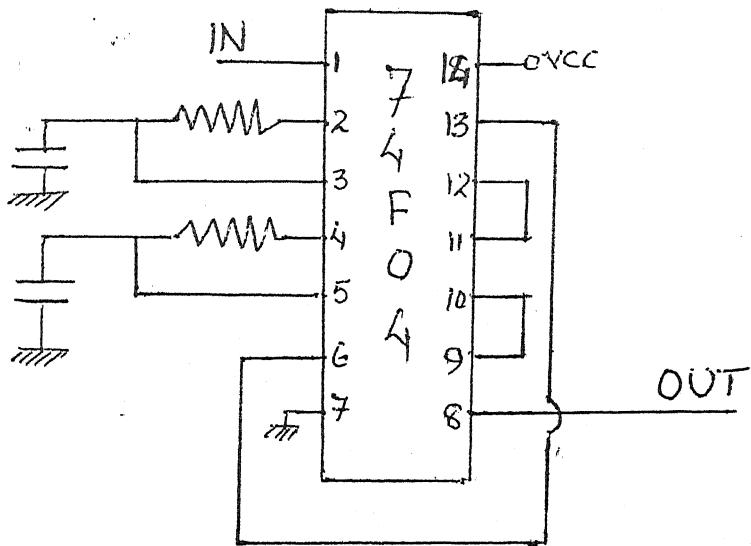
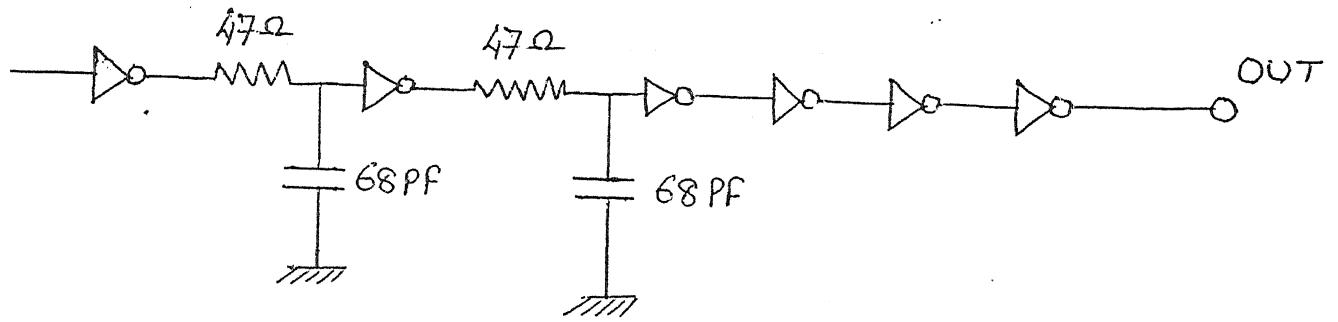
3.4.2.1 PREAMBLE BIT GENERATION

As soon as data is received in the ESI chip CRS ie, carrier sense signal goes low after 100 n sec. Then after 1400 n sec it gives RXC clock and data RXD. During this 1400 n sec or 14 clock cycles the first 12 to 14 bits of data are lost which are nothing but a sequence of 10101010... as preamble bits. So there is a need in the repeater to get these bits generated and passed to output first and then the actual data should follow. In any case the total preamble bits out from repeater should be equal to or more than 56 bits. So the first 20 bits of 1010... generated in preamble generator were passed through output MUX to output ESI and then the main data was selected to pass over.

3.4.2.2 BUDGETING FOR DATA READ

Proper care should be taken to read the data from FIFO at a particular moment of time. For this the following calculation was made:

As per IEEE 802.3 standard the clock must be of 10MHz $\pm 0.01\%$. So in worst case these two clocks RXC and TXC will have a maximum difference of 0.02 % creating a shift of one clock cycle slip in 5000 cycles. Which is around 600 bytes of data. So there is a chance of slip of one cycle in these two clocks after 600 bytes of data transfer in worst case. So taking the maximum frame size of 1518 bytes there will be atmost three cycles slip in worst case. At the same time the



latency for read and write is one clock cycle for FIFO so total of four clock cycles slip is possible to occur. If the error is more but in limit then chances of more cycles slip is also possible. Hence an agreement was made that the read clock of FIFO lags by four cycles to write clock in the begining. So even if there is a positive slip the read address will not catch the write address at the end of full sized frame transfer or in case of negative slip will not give a gap of more than 7 addresses between read and write address. This satisfies the IEEE standard which states that the maximum in/out delay should be 7.5 bits of time at the begining and 9 bits of time at the end of frame transfer. To achieve this when the CRS signal goes low, was first given a shift of four in the shift register (74F164) and output was muxed with 8 clock shift of the same. The 8 clock shift was taken into account to give sufficient time for reading of data and whole system to get reset after the end of frame. As at the end of data CRS goes high and hence after 8 cycles delay the same signal is used as reset pulse to all concerned chips known as SYSCR.

3.4.2.3 CONTROL SIGNALS

The CRS when goes low after a delay of 4 cycles starts outputing a counter. At the count one the preamble generation starts and goes as input to the MUX and then to output ESI.

As almost at 13 cycles of RXC delay from CRS activation the RXD data starts pouring in to the FIFO, so on the count of 13 the read pulse ie, TXC was made to start reading the FIFO. This way the FIFO was made to be read after $13+4 = 17$ cycles of CRS activation giving a latency of 4 cycles between read and write in the begining. The read data was compared with the generated preamble data in

MUX was given a select signal at the count of 20 to get the data of main data path. The count 20 was chosen randomly allowing the stabilisation of data at the input of output MUX.

This way the generated preamble bits were driven out first hence the lost preamble bits were regained.

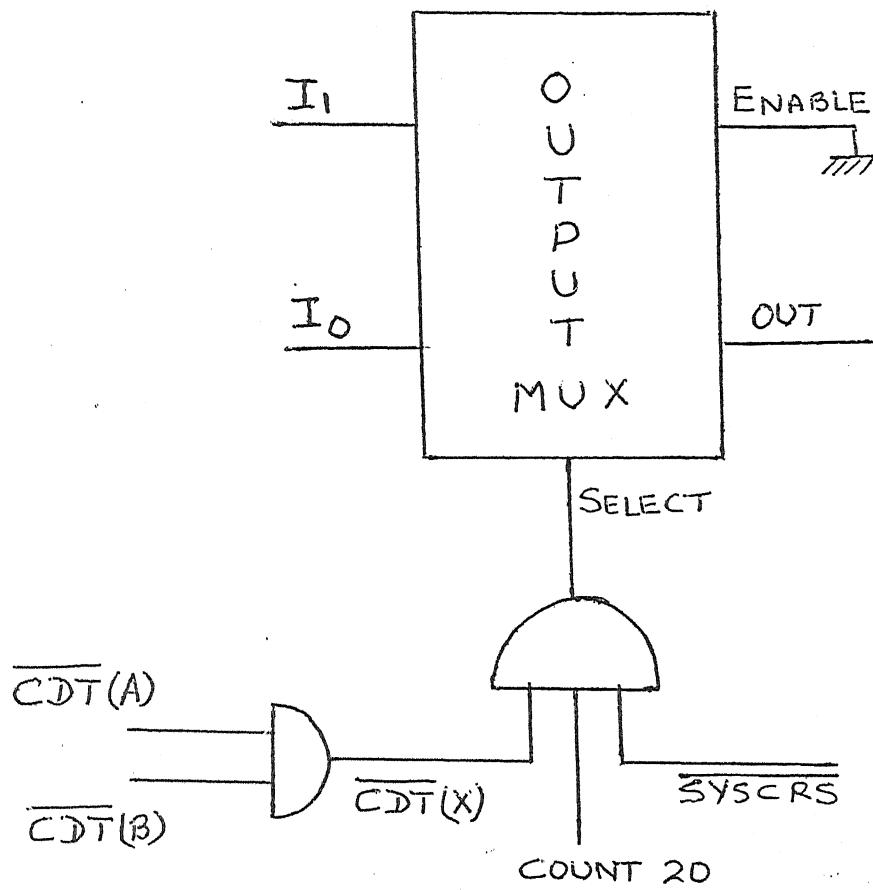
3.4.3 Collision and Jam Signal Generation

3.4.3.1 COLLISION DETECTION

When the 10 M Hz signal is received at CLSN pair of ESI this asserts CRS low and CDT low. There is a provision that if NOOR of ESI is pulled high permanently only then CRS and CDT both will go low. If NOOR is pulled low then only CDT will go low. In our case NOOR was pulled high and CRS and CDT both the signals were used for JAM generation.

3.4.3.2 JAM GENERATION AND OUTPUT

(A) When collision signal is received at input of repeater: The low CDT signal inhibits the selection of output MUX as in fig. 3.6. Due to the CRS going low the usual preamble generation starts and goes out to output MUX and then to output ESI. As the selection is always set to zero due to low CDT only preamble bits as 101010... keeps going to output ESI. If the CRS/CDT goes high after a few μ sec even then the MUX is not selected for other input as SYSCRS then goes low and the selection is inhibited. The CDT of one side also activates the SYSCRS of other side as shown in block



ENABLE	SELECT	OUTPUT
Low	Low	I_0
Low	High	I_1

SELECTION OF OUTPUT MUX

FIG. 3.6

Hence 10101010... goes as output to both the sides of repeater creating a JAM signal on the network.

(B) When the repeater is outputing and at the same time transceiver gets data from other side: In this case the output of repeater when goes to transceiver and as usual loops back in it, the transceiver senses a collision and starts sending a collision to the other side of the repeater. This signal activates the CRS and CDT signal at the ESI of other side. This CDT signal inhibits the selection of output MUX at both sides and causes a JAM signal output to both sides.

In our design this common CDT signal has been named as CDT(X) which is nothing but ANDing of both side CDTs. The generation of 101010... stops at the count 98 and the whole system comes to a reset condition.

3.4.4 *Fragment Extension*

If a very very short packet i.e., less than 96 bits is received then it is the duty of repeater to make it up for 96 bits. For this the count of 98 of the counter was used. The counter keeps counting upto 98 and then stops the counter and resets the flip flops so that the preamble generator stops generation.

The care was taken with the SYSCRS signal which inhibits the selection of output MUX if CRS is pulled up due to a short packet. The MUX selection comes to 10 and 10101010... are still transmitted to output ESI, thus compensating for rest of the 96 bits. The 98 count was accounted to keep the repeater output carry on for 9.8 μ sec meeting the requirement of IEEE standard.

Chapter 4

HARDWARE DETAILS

4.1 DETAILS OF CIRCUIT

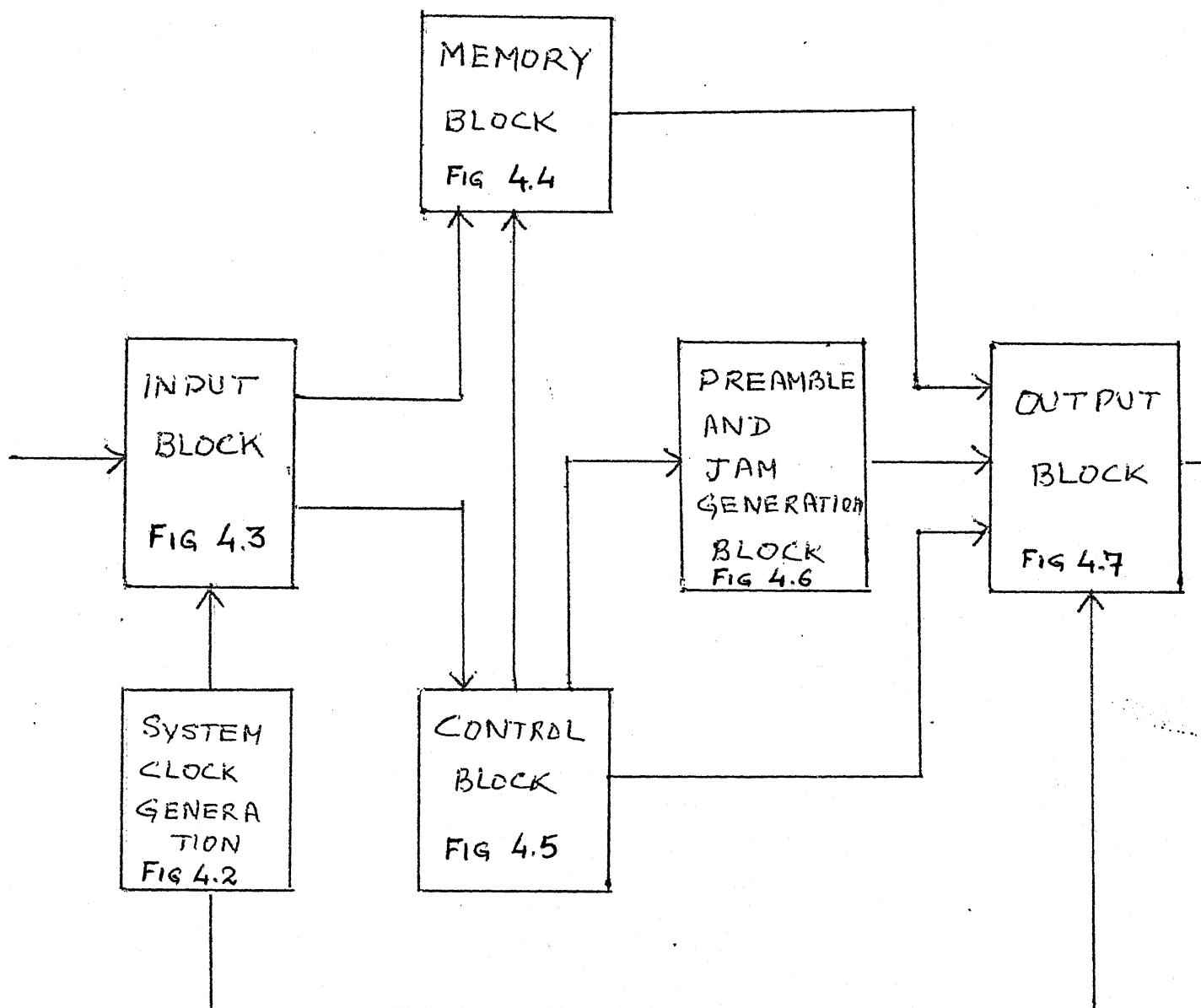
The circuit was divided in following blocks as shown in fig. 4.1:

1. System clock generation
2. Input block
3. Memory block
4. Control block
5. Preamble and Jam Generation
6. Output block

4.1.1 System Clock Generation

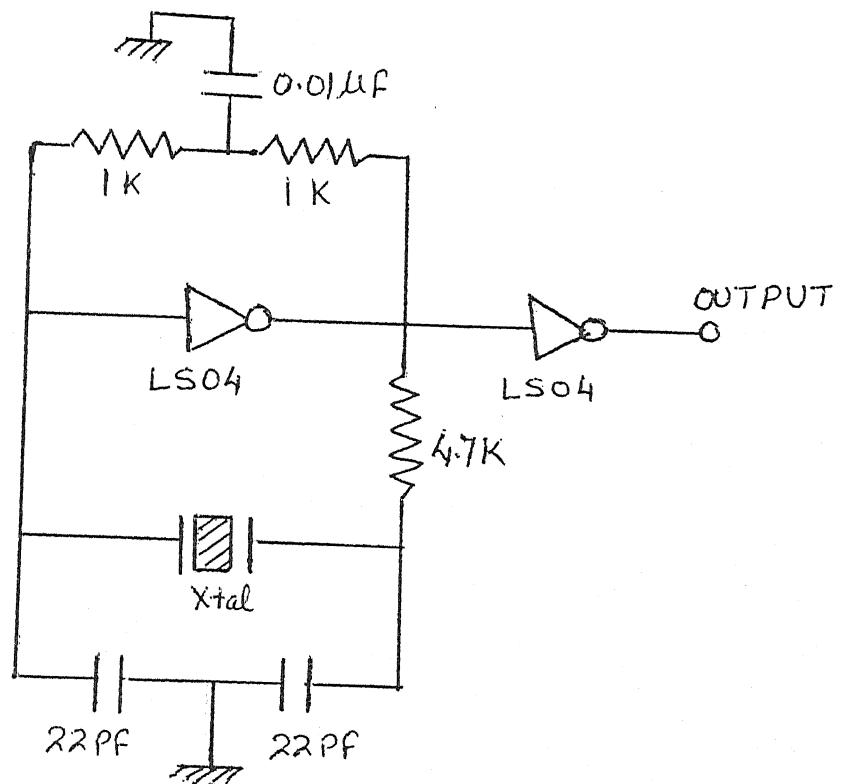
A 20MHz crystal was used to fabricate one oscillator circuit as shown in fig. 4.2.

The 20 MHz output of this circuit was fed to the X1 input of each ESI chip ie, both sides of repeater. This 20 MHz is divided by two in the ESI and this 10 MHz clock was termed as system clock for each sides . This system clock is known as TXC of each sides, these are continuously running clock as soon as the power to the repeater is on.



BLOCK DIAGRAM OF REPEATER

FIG 4.1



20 MHz OSCILLATOR

FIG. 42.

4.1.2 Input Block

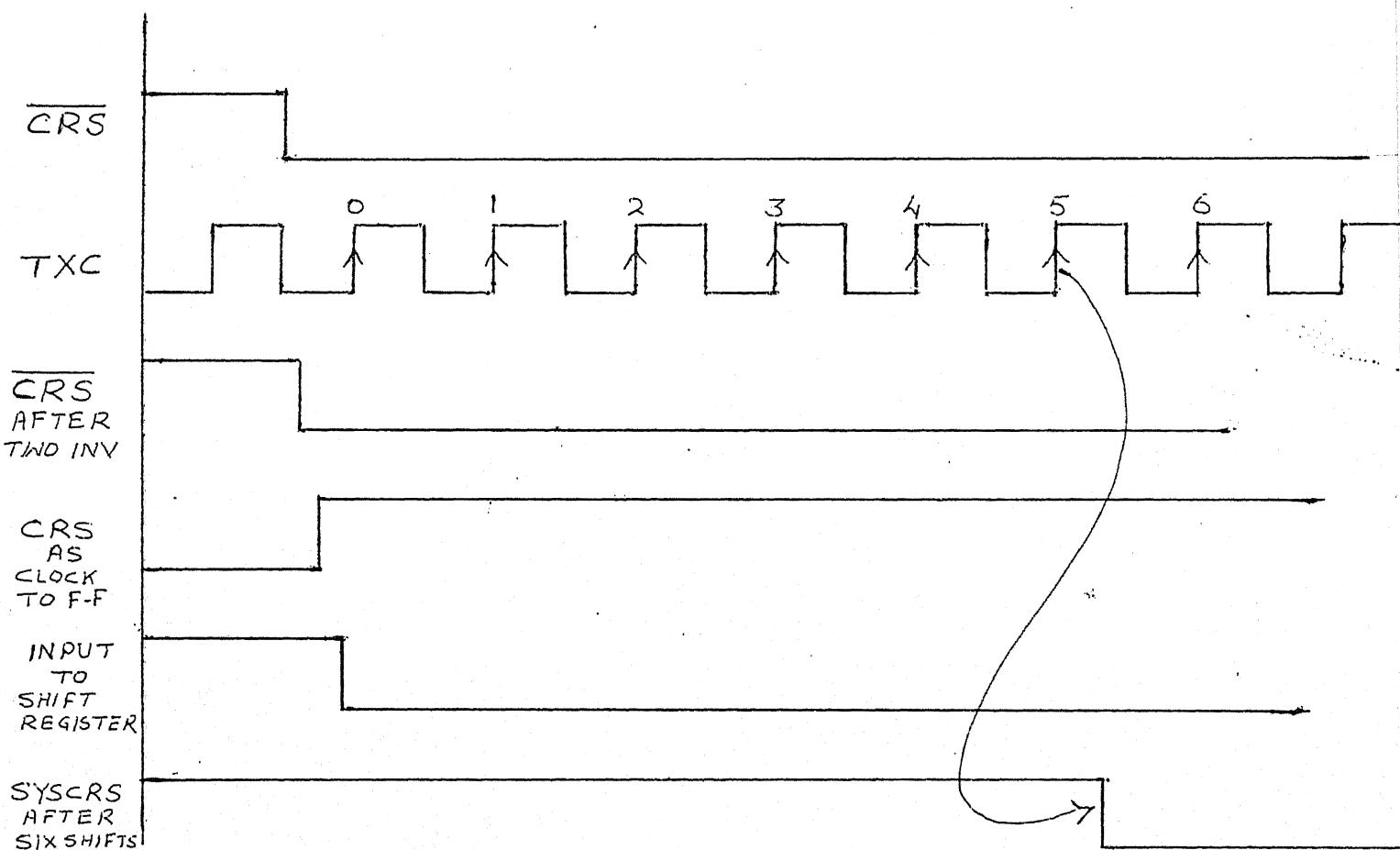
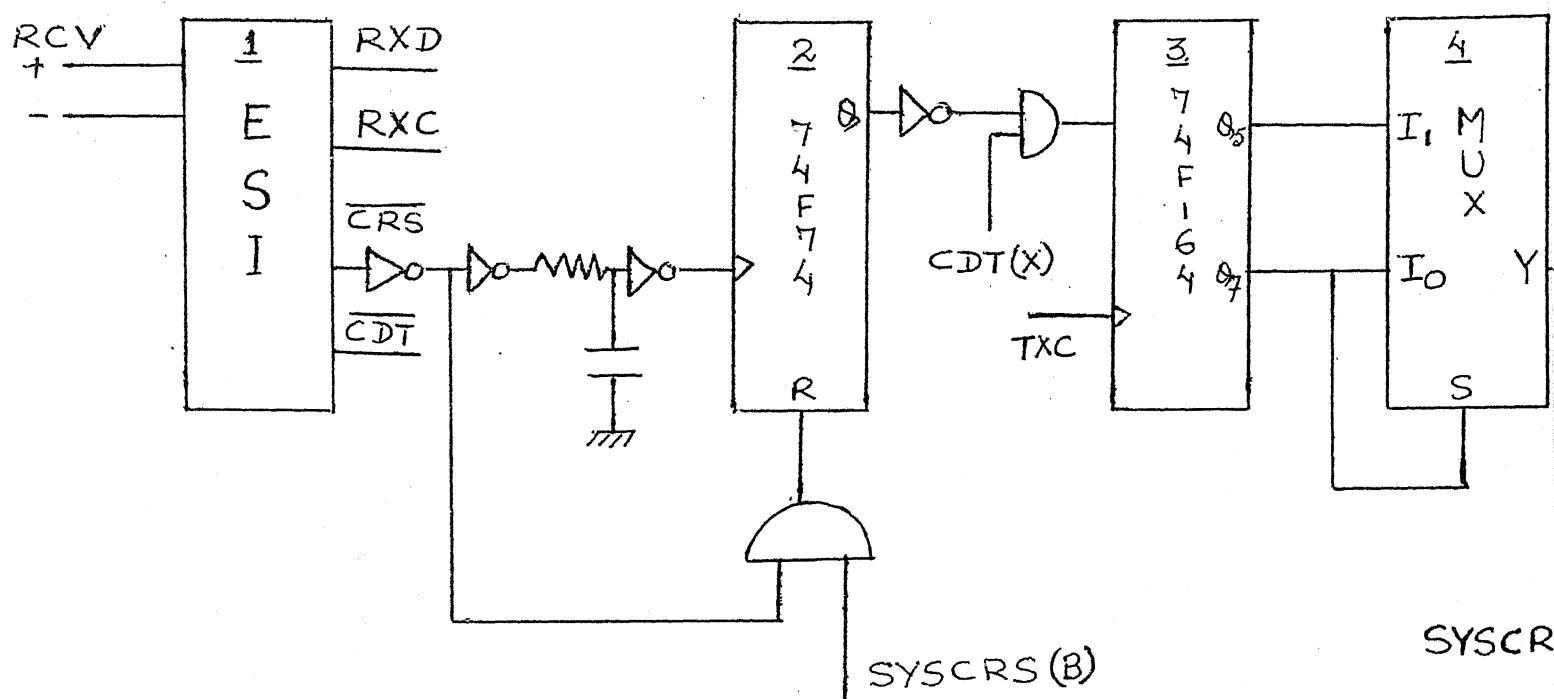
This is shown in fig. 4.3. The data is received at RCV pair of ESI chip. It gives out CRS low. This CRS low is given as reset input to a flipflop. 2. through an AND gate which has the other input as SYSCR_S of other side so that if the data received is a loop back data of transmitted data from the same side, will inhibit this AND output and hence the flipflop will remain in reset condition causing no further move of CRS. This side ESI will keep transmitting until unless the SYSCR_S of other side goes high. When the SYSCR_S of the other side is high then CRS of this side goes further and the flipflop 2. latches to a high level. It is then inverted and ANDed with CDT(X), as CDT(X) is high if there is no collision sensed, then this low output of AND is shifted four times with the help of TXC clock in the shift register. It is also given 8 shifts and muxed. The output of MUX is known as SYSCR_S. The same is inverted and known as SYSCR_S.

The data is decoded in NRZ form and catered for noise filtration as well as amplified in the ESI chip.

4.1.3 Memory Block

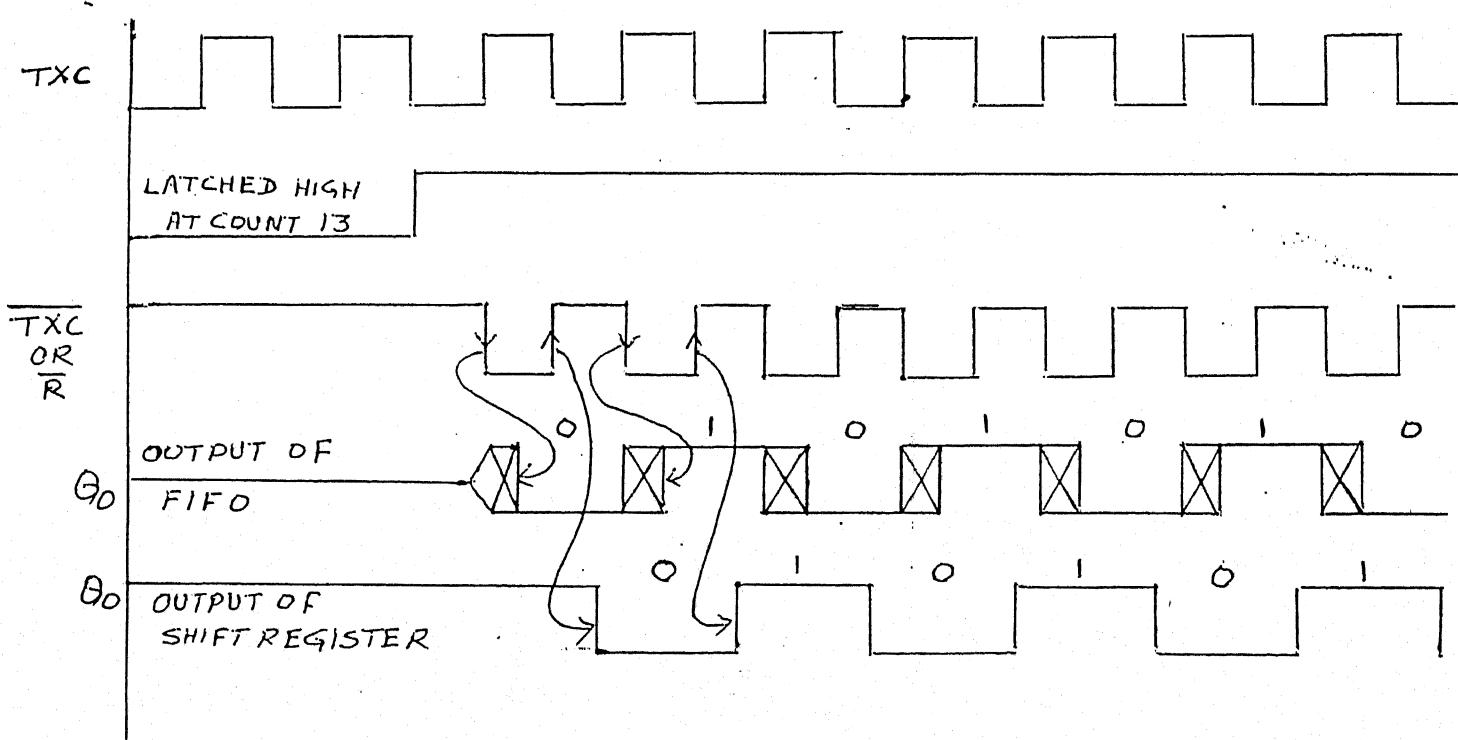
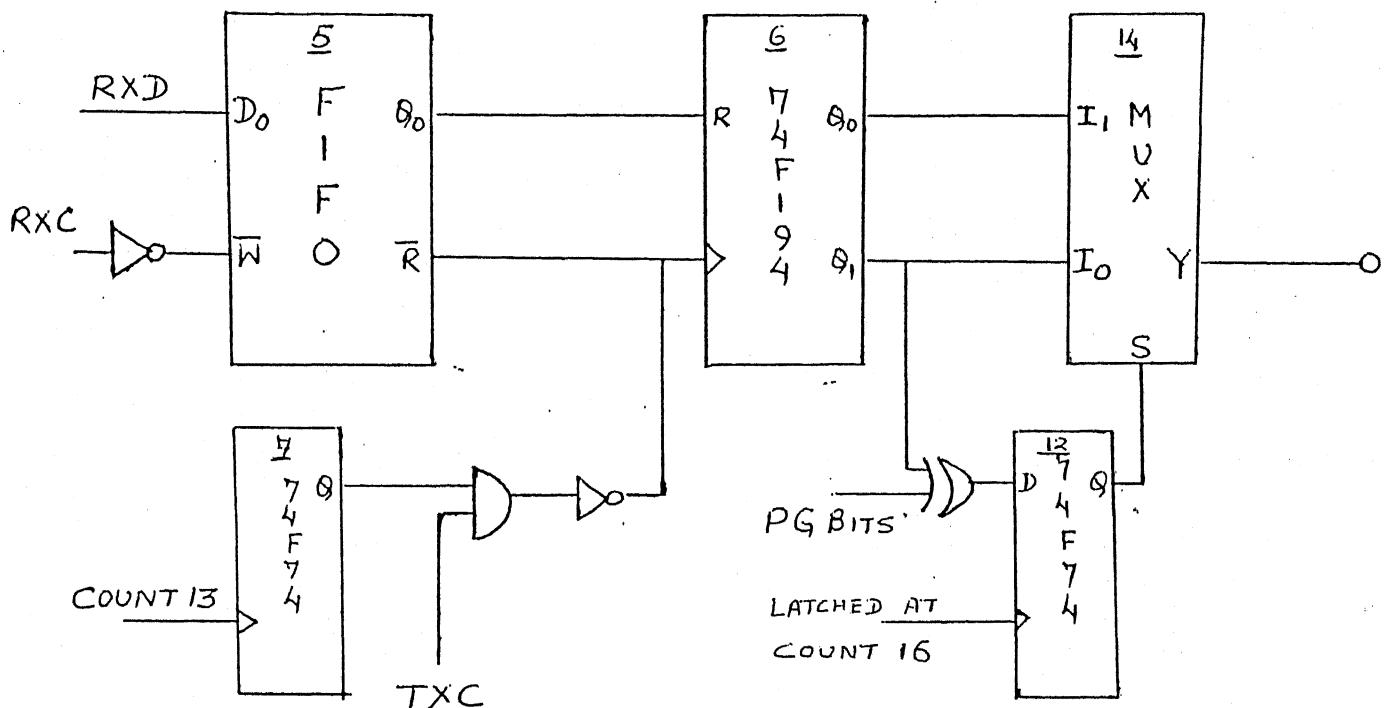
The RXD data is stable at the negative edge of RXC but to write in FIFO it should be stable at positive edge of clock so RXC was inverted and given to FIFO along with RXC. After 1300 nsec of CRS activation data was written in FIFO from zeroeth location onward. The details are shown in fig. 4.4.

The same was read with TXC clock at the count of 13. The flip flop 7. latched a high level at count 13 and so the AND gate was enabled and TXC clock was made to pass to FIFO after inversion.



INPUT BLOCK AND TIMING DIAGRAM

FIG 4.3



MEMORY BLOCK AND TIMING DIAGRAM

FIG 4.4

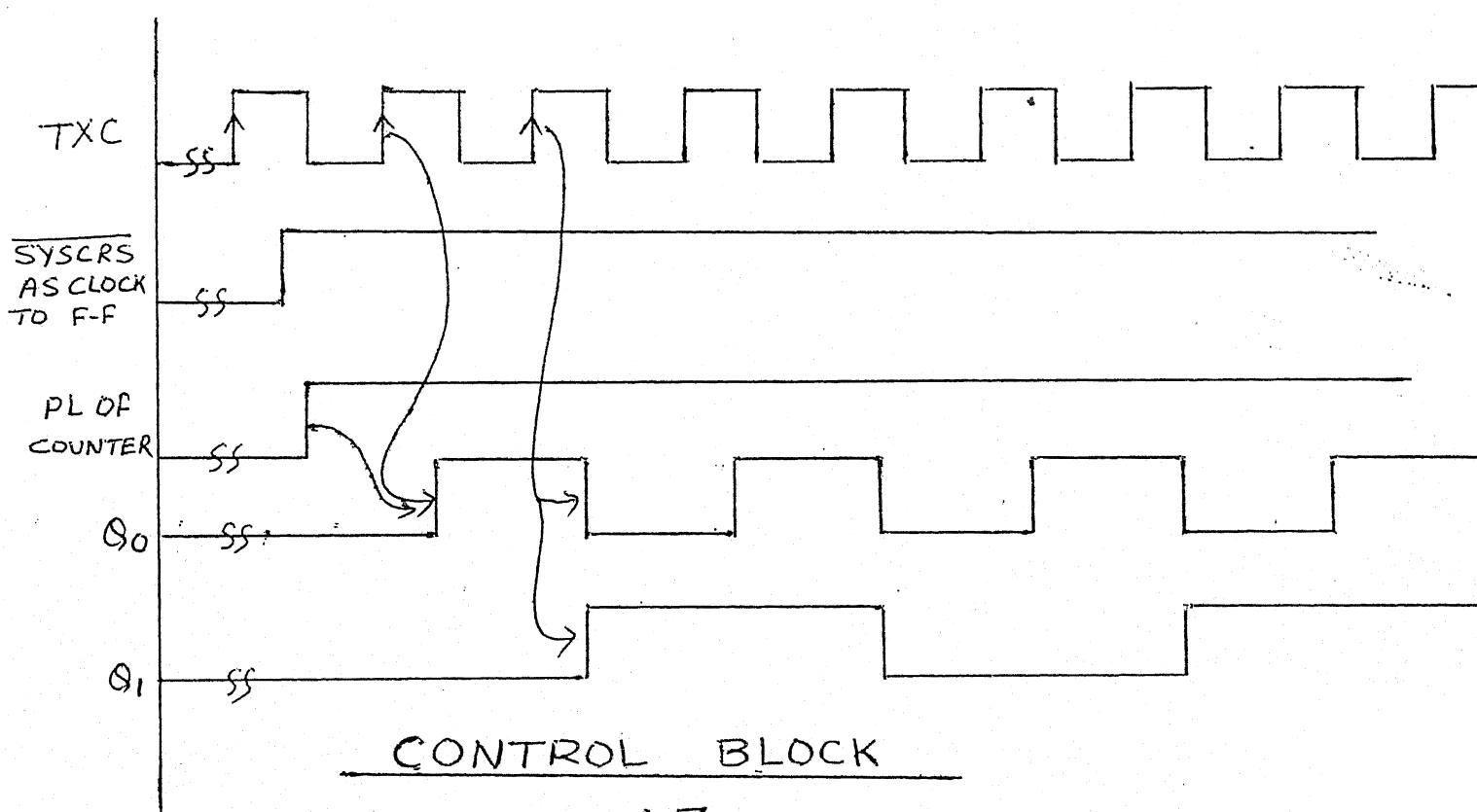
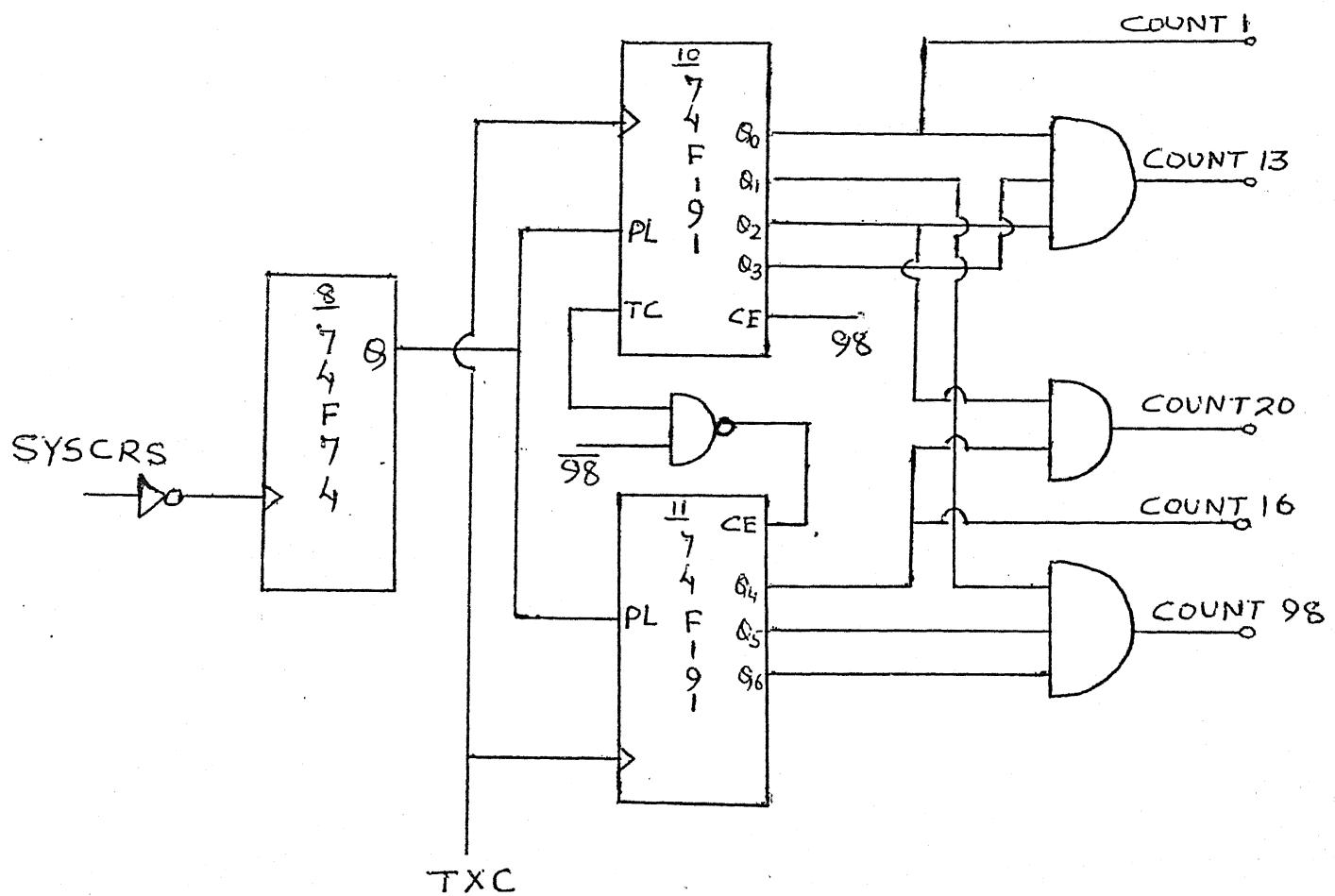
The FIFO has the main criteria that when reset input is going high the read and write clock should be positive. Hence these inversions in TXC and RXC solved this problem.

Shift register 74F194 shifts the data by one clock cycle at Q0 and by two clock cycles at Q1. The Q1 data is compared with generated preamble data with the help of EX-OR gate and output is latched through flip flop.12. to select the correct phase of data to go out to output MUX.

4.1.4 Control Block

The control block is the heart of the repeater. It has following parts as shown in fig. 4.5:

- (1) Both the CDTs of these two ends are ANDed and output named as CDT(X) is fed to both side AND gates which is responsible to give the input to the counter.
- (2) The counter starts counting as soon as PL input to this is high due to SYSCRS. The low to high transition of SYSCRS latches the high level to PL and counter starts its operation with the help of TXC clock.
- (3) At count one the low to high transition latches the high level in flip flop.13. which then goes as reset input to JK flipflop which then starts giving output as 101010... as half of the TXC clock making the same form of data like RXD. This output goes to output MUX.
- (4) At count 13 data is read from FIFO.



CONTROL BLOCK

FIG 4.5

(5) At count 16 the flipflop.9. latches a high level transition to another flip flop.12. which then latches a level depending upon the output of EX-OR. This output of flip flop.12. then selects the MUX to get the in phase data from shift register.

(6) At count 20 flip flop 16 latches a high level to the select input of output MUX and then data RXD goes out to the out put ESI.

(7) At count 98 the counter itself resets and the flip flop.8. and 13. are also reset to stop the preamble generation further.

4.1.5 Preamble And Jam Generation

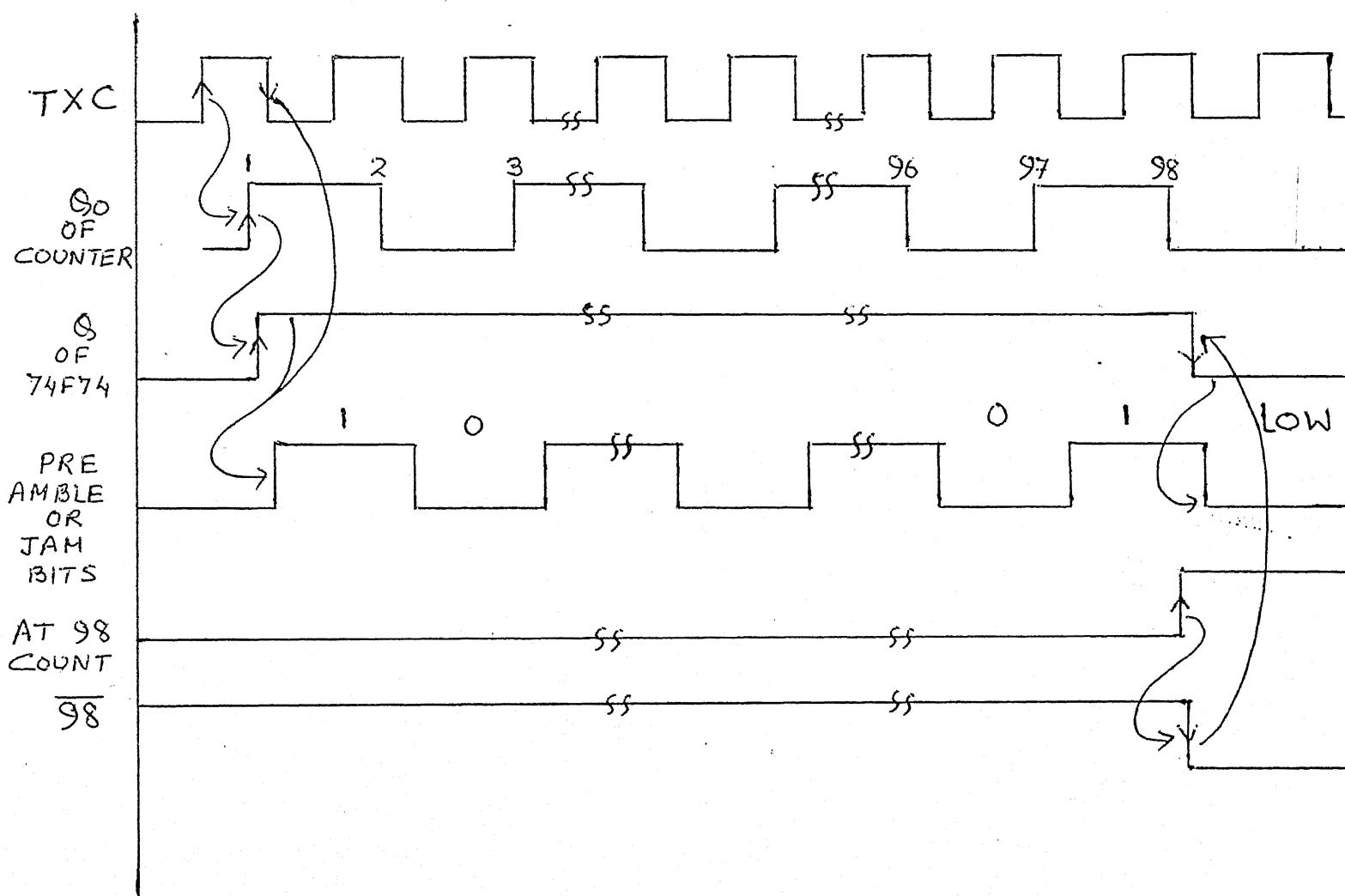
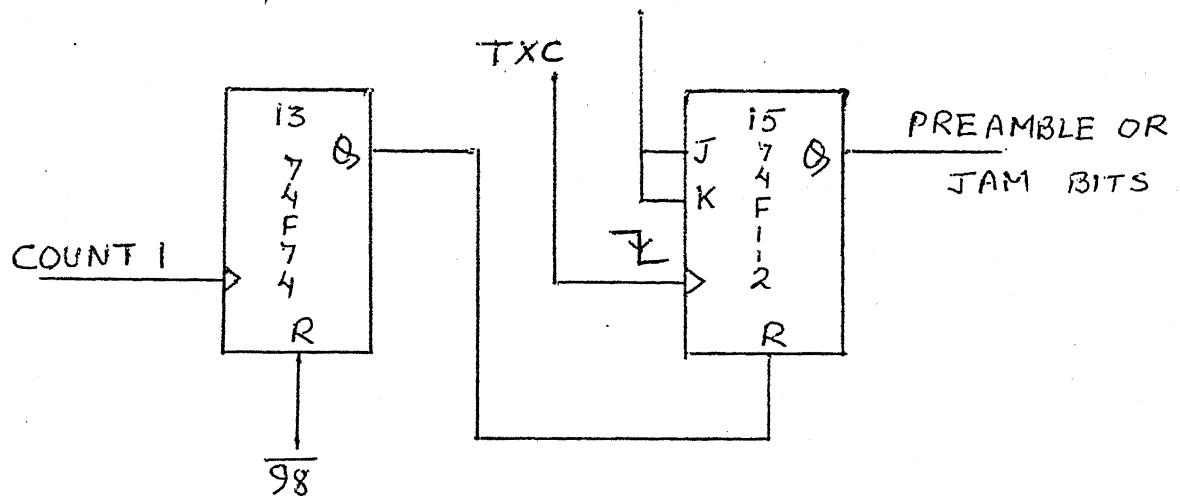
This block consists of one flip flop 74F74 and a JK flip flop 74F112 which are positive and negative edge triggered respectively. The details are shown in fig. 4.6.

At the count 1 of the counter the flip flop 13 latches high signal as reset to JK flip flop 15. Then the flip flop starts toggling at half the frequency of TXC and 101010... comes as output at Q0 of it. This data is treated as preamble or jam bits according to the control signals.

4.1.6 Output Block

The output block consists of output MUX, a delay circuit and output ESI as shown in fig. 4.7.

(1) Output MUX is only flipping the path of generated preamble data to the main RXD path at count 20.



PREAMBLE AND JAM GENERATION

FIG 4.6.

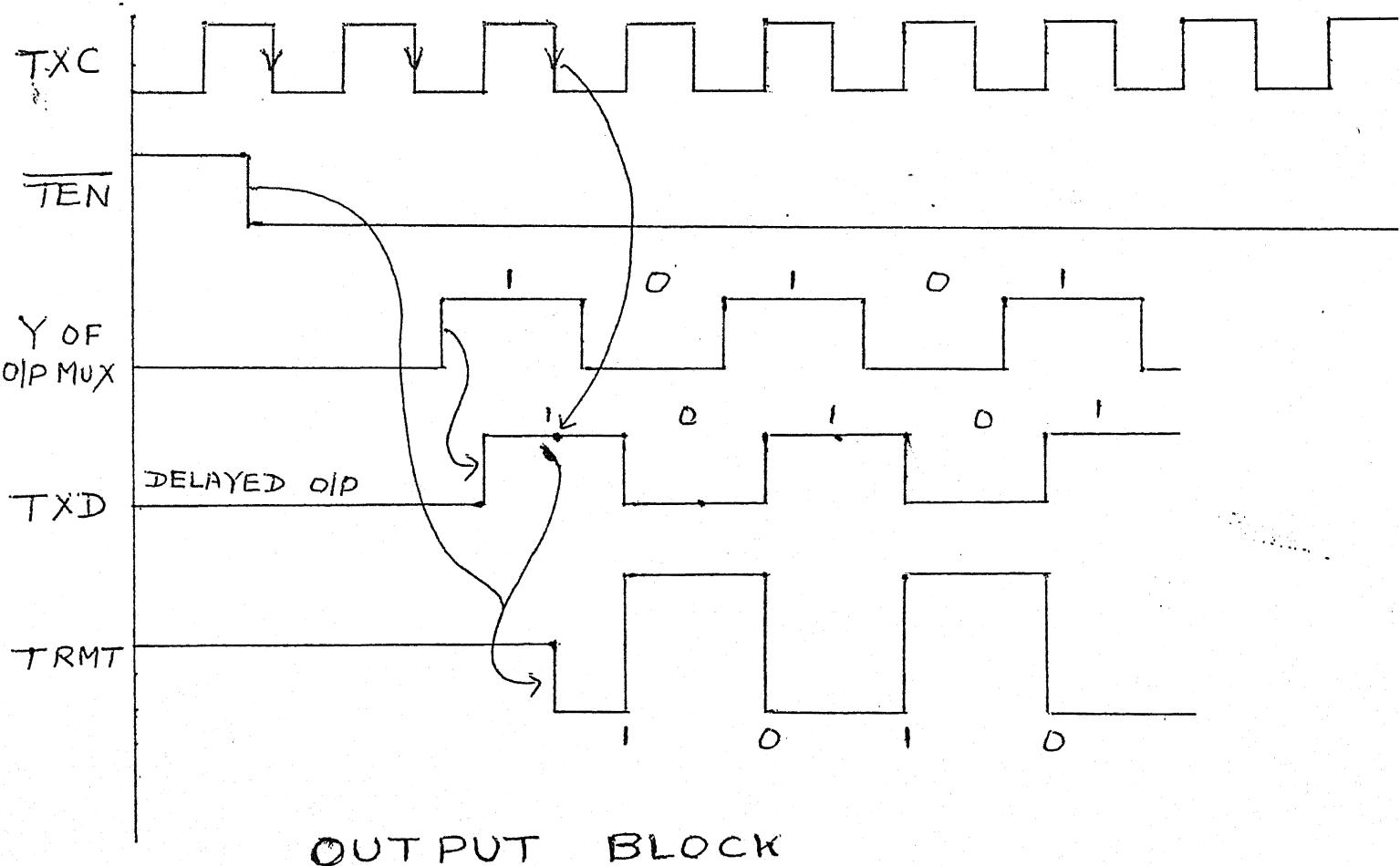
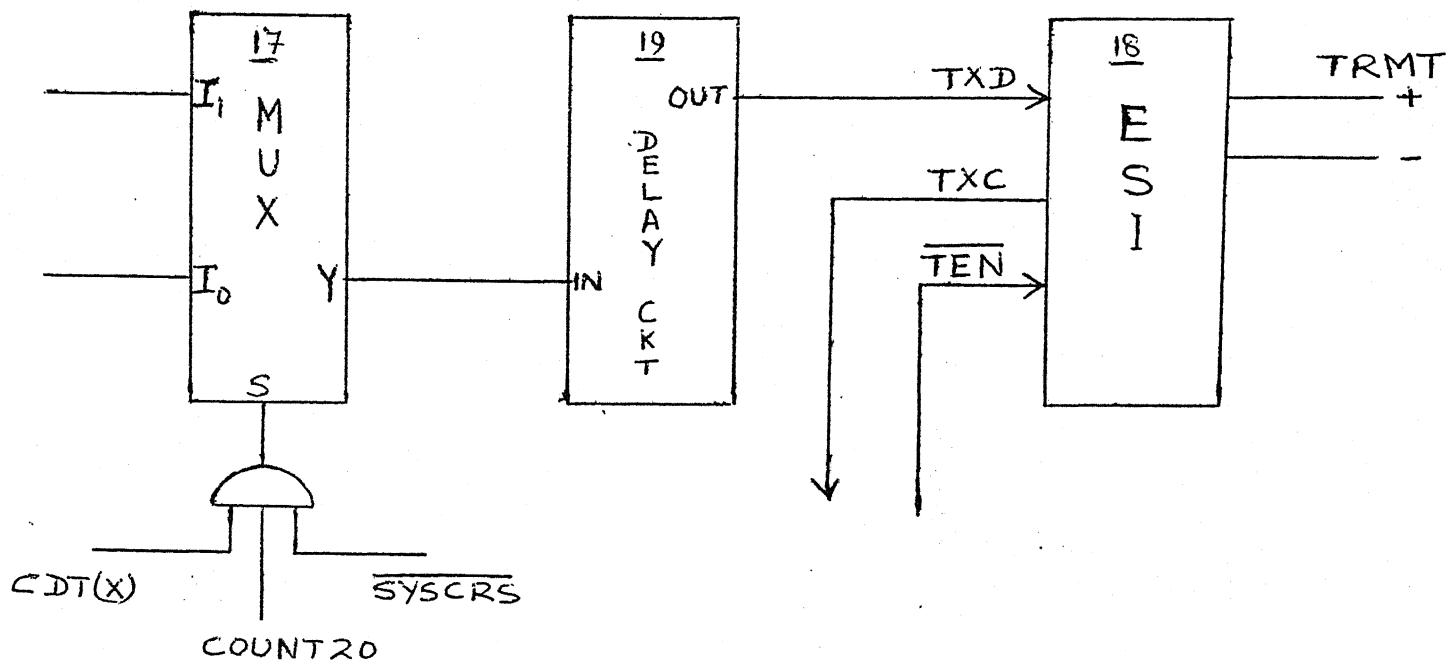


FIG 4.7

(2) The delay circuit gives a delay of about 25 nsec so that data RXD now TXD is stable at the negative going edge of TXC. Hence the ESI can further encode the data to manchester form.

(3) Output ESI encodes the data to manchester form as well as restores a proper level for onward transmission.

(4) The TEN signal should be low for data output at output ESI so SYSCRs is used as TEN signal after ANDing with latched output of 98 count. This helps in enabling the transmission in case of collision or fragment extension. As during normal valid data transfer the SYSCRs will be low till the full packet is passed over causing the TEN to be low.

4.2 COMPLETE CIRCUIT AND TIMING DIAGRAMS

The complete circuit details and the different timing diagrams are shown in figs 4.8, 4.9, 4.10, 4.11 and 4.12. The fig 4.8 shows the data transfer from left to right and fig. 4.9 shows from right to left. These circuits were fabricated on only one wire wrap board. The oscillator circuit was common for both the circuits. The X1 inputs of both the ESIs were given the output of oscillator circuit of 20 MHz. figs. 4.10, 4.11 and 4.12 give the complete timing diagrams and delays of the repeater for one side operation.

REPEATER FOR ETHERNET \Rightarrow

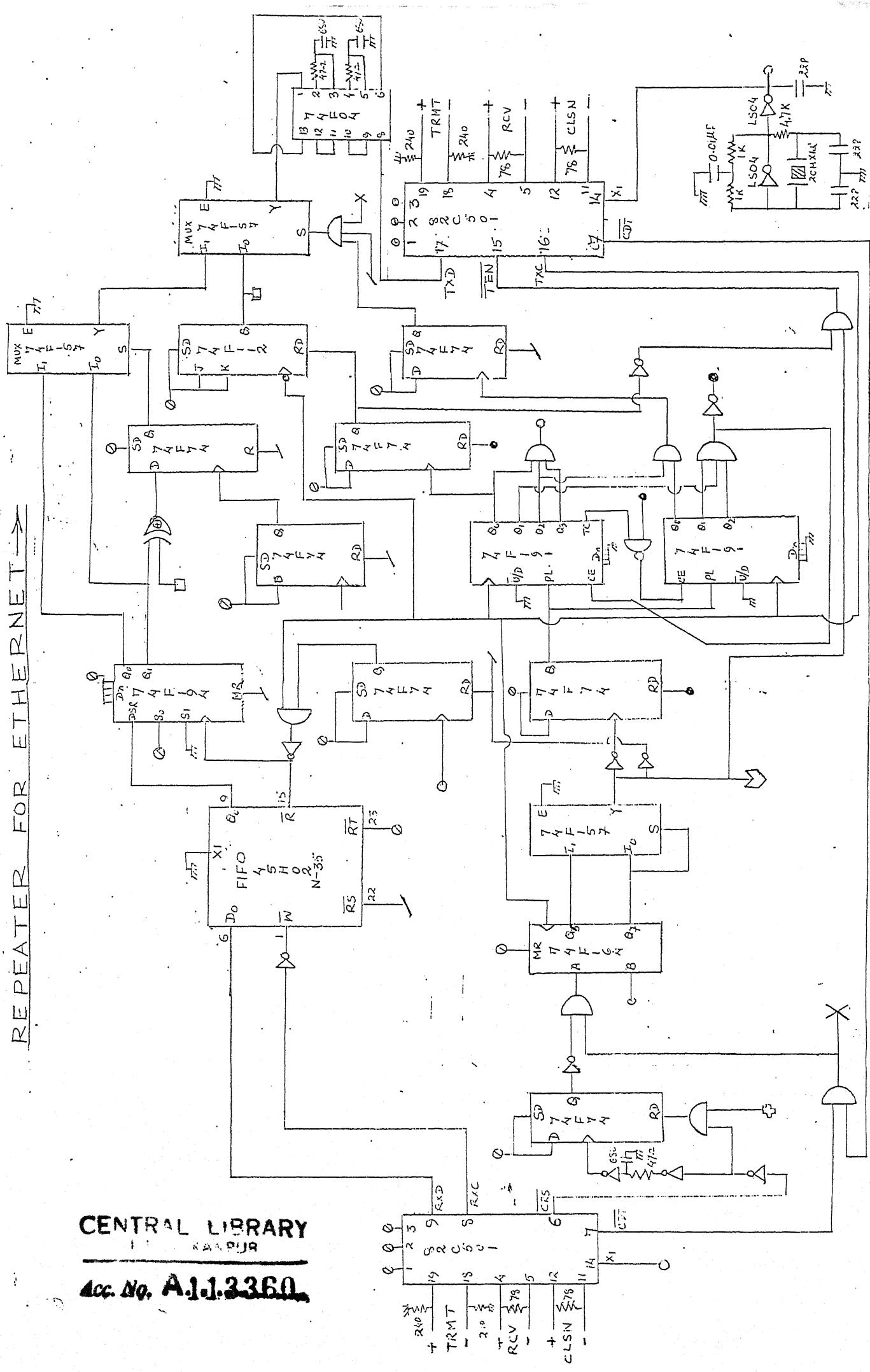


FIG. 4.8

← REPEATER FOR ETHERNET

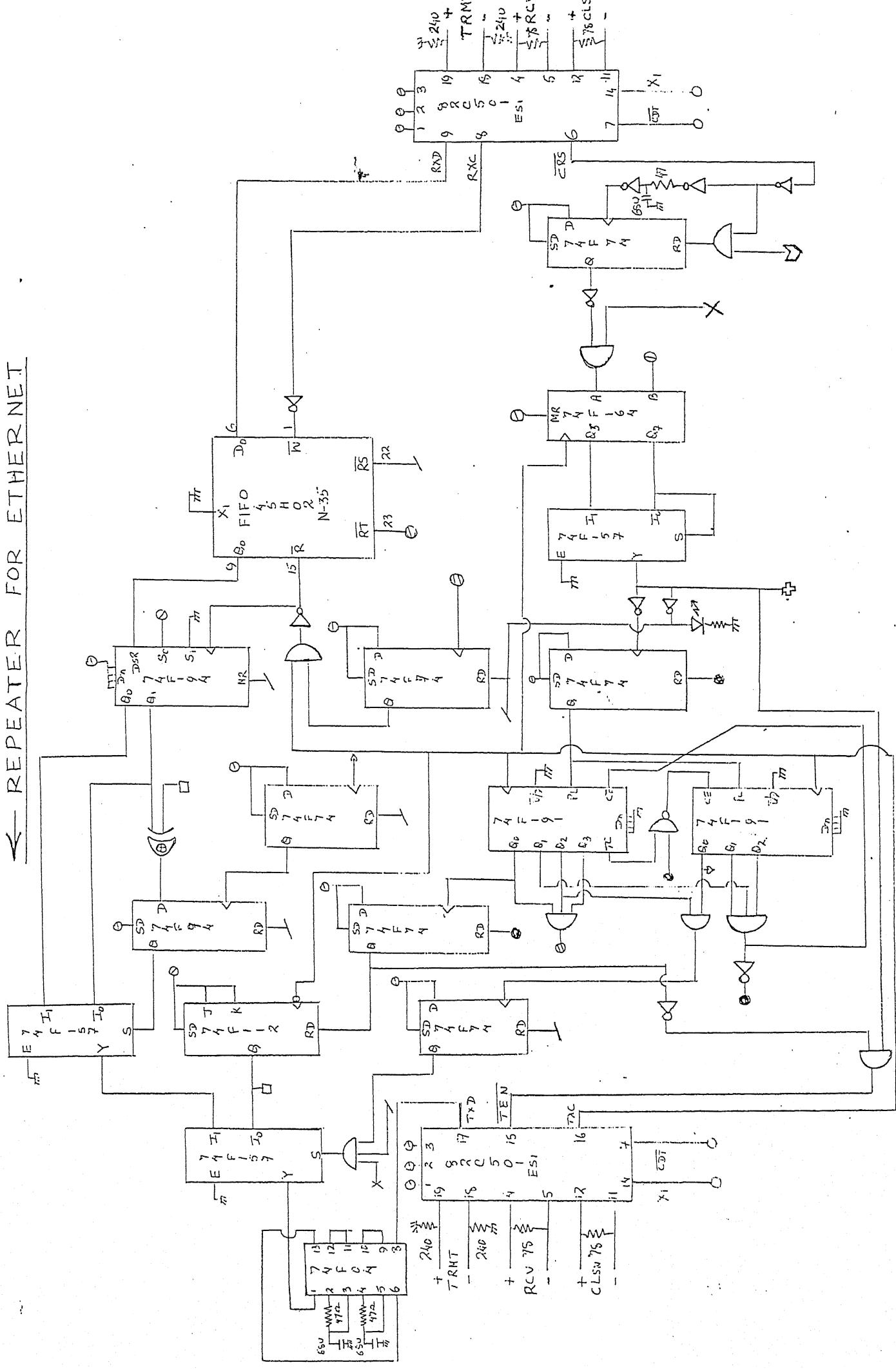
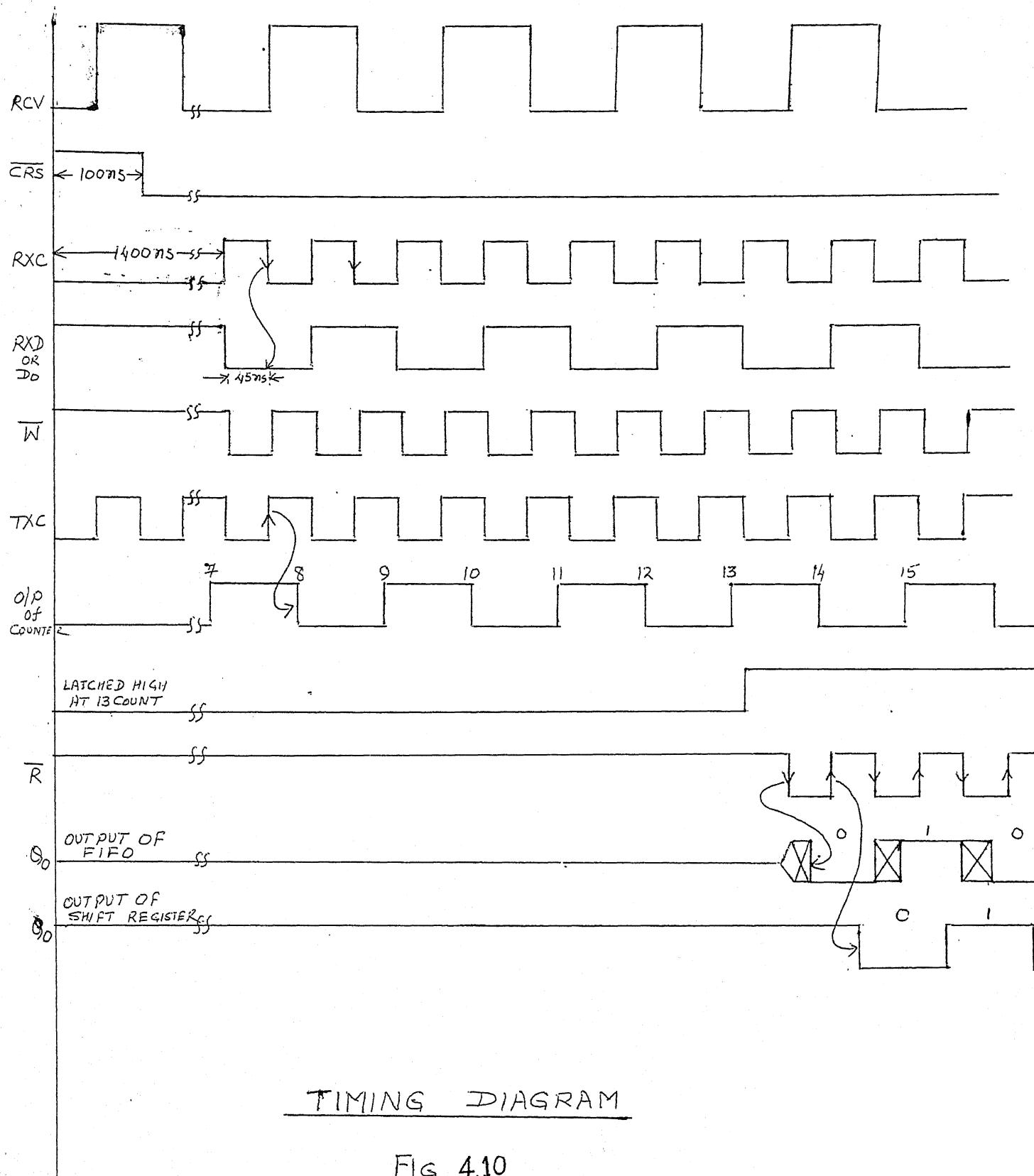
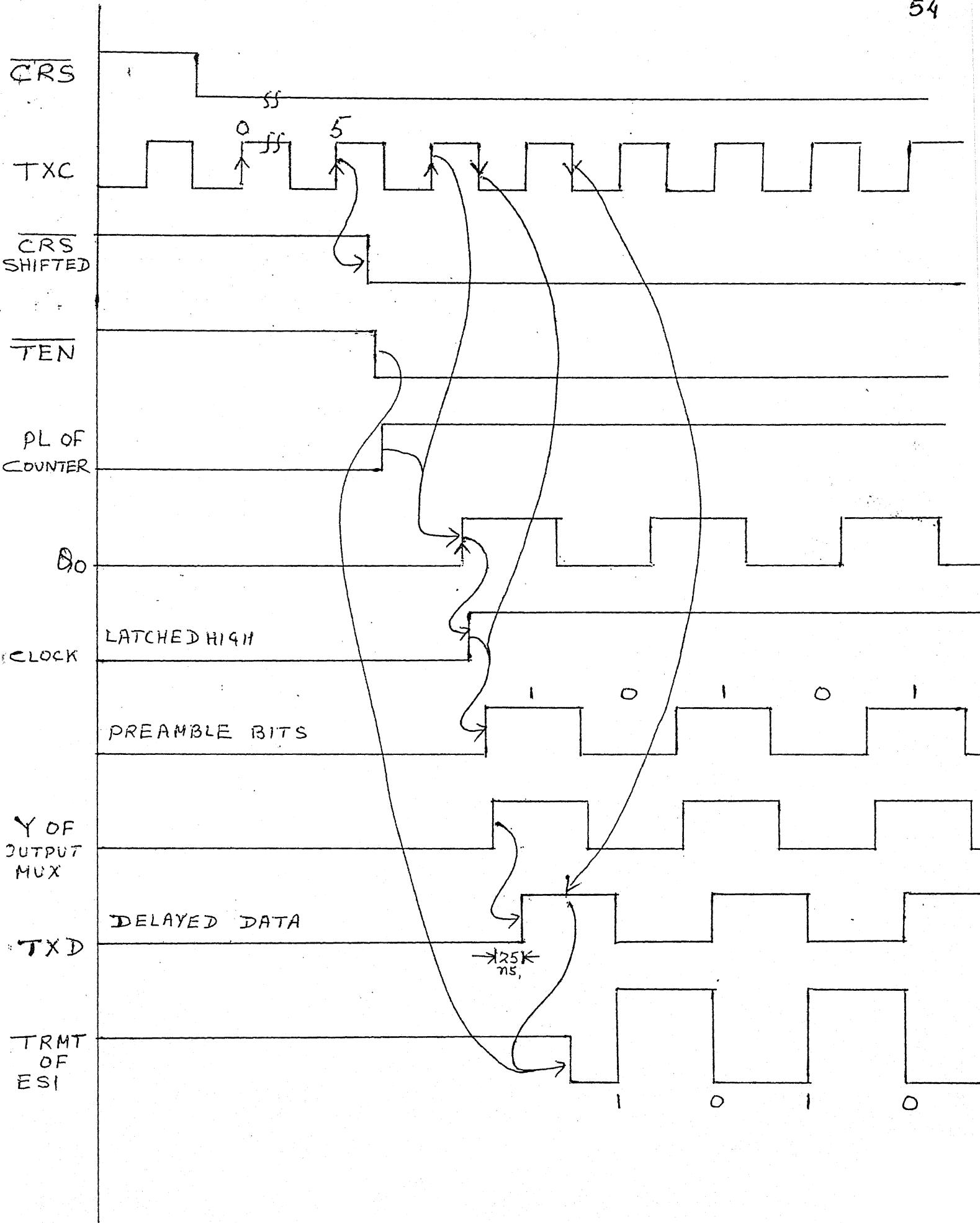


FIG. 4.9



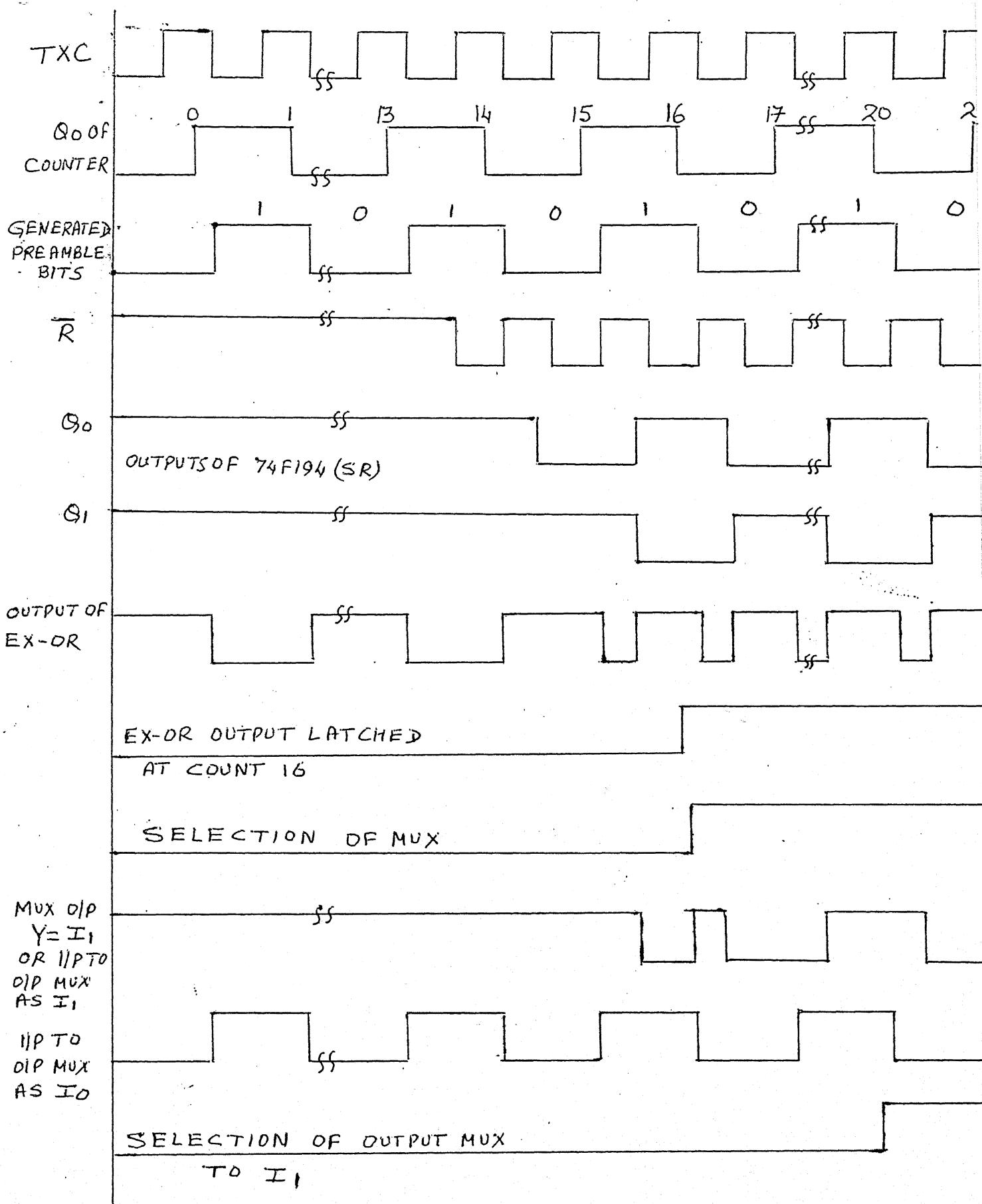
TIMING DIAGRAM

FIG. 4.10



TIMING DIAGRAM

FIG. 4.11



TIMING DIAGRAM

FIG 4.12.

Chapter 5

PERFORMANCE AND CONCLUSION

5.1 FABRICATION

The circuit was fabricated block by block on a wire wrap board. On line checks were carried out to test the functions of each block. Firstly only the circuit for one direction was assembled. The circuit was tested by using slow clock and then operated at the specified clock of 10 MHz. The circuit for the other direction was subsequently assembled and integrated. The system was verified for functionality over the LAN Test Bed.

5.2 THE TEST SET-UP AND THE PERFORMANCE CHECK

The circuit was tested on a test set up as shown in fig. 5.1. Textronics TC 2000 Protocol Analyser was used to monitor the output of Repeater. The Analyser collects all the packets available on the network and can be analysed for the size of the packets i.e., no of bytes, short packets and the errors in the packets such as CRC/ALGN error or collision error. The input was given from a PC on which a test program was run over PC-IP (TCP/IP protocol for PC). The test program is a Local Area Network Traffic Generator (LTG) program which has been implemented recently under ERNET Project. The LTG program could be simulated with varying

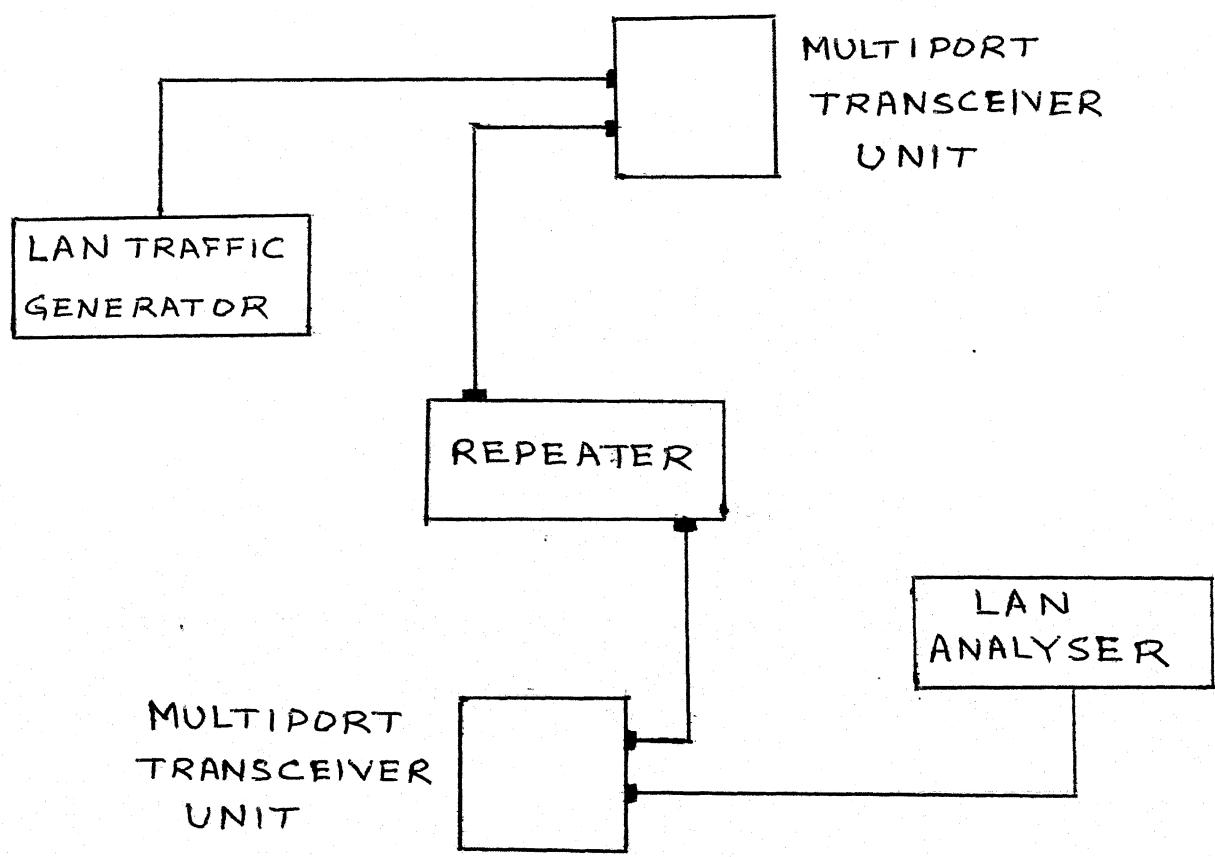
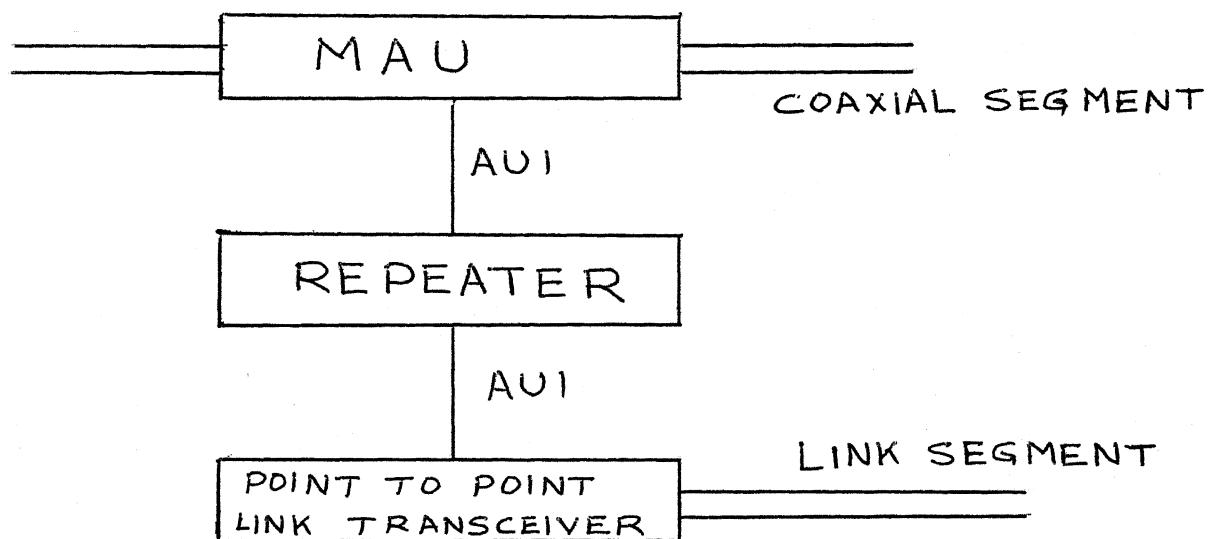


FIG 5.1

packet sizes from 48 bytes to 1500 bytes and varying repetitive information bits. It also had the provision to vary the inter frame spacing starting from 9.6 μ sec to infinity. The Repeater worked satisfactorily with no errors at different sizes of packets. The performance curve has been shown in fig. 5.2. The first curve shows the nature of the packet size and the packet rate at the output of the LTG. The second curve shows the nature of that at the output of the Repeater. It was observed that due to the limitations of the software in LTG, at the packets of low bytes only 6000 packets per second could be output from the PC instead of ideal 16000 packets per second. But the packet rate at the input and the output of the Repeater remained same and there were no loss of packets in it during the packets transfer. Even no erroneous packets were received at the output of Repeater.

Occurrence of collision was also verified by enabling SQE switch of the Multiport transceiver unit. When SQE is enabled a collision test signal of 10 MHz for 5 to 15 bits time is generated at transceiver unit which causes the Repeater to send out 101010... for 96 times to both the sides. It was observed on a 275 MHz oscilloscope.

5.3 PERFORMANCE ON NETWORK

The repeater was installed on the campus network as shown in the fig. 5.3. All network services on PC was found to be satisfactorily working on main network. The data transactions were without errors and delays.

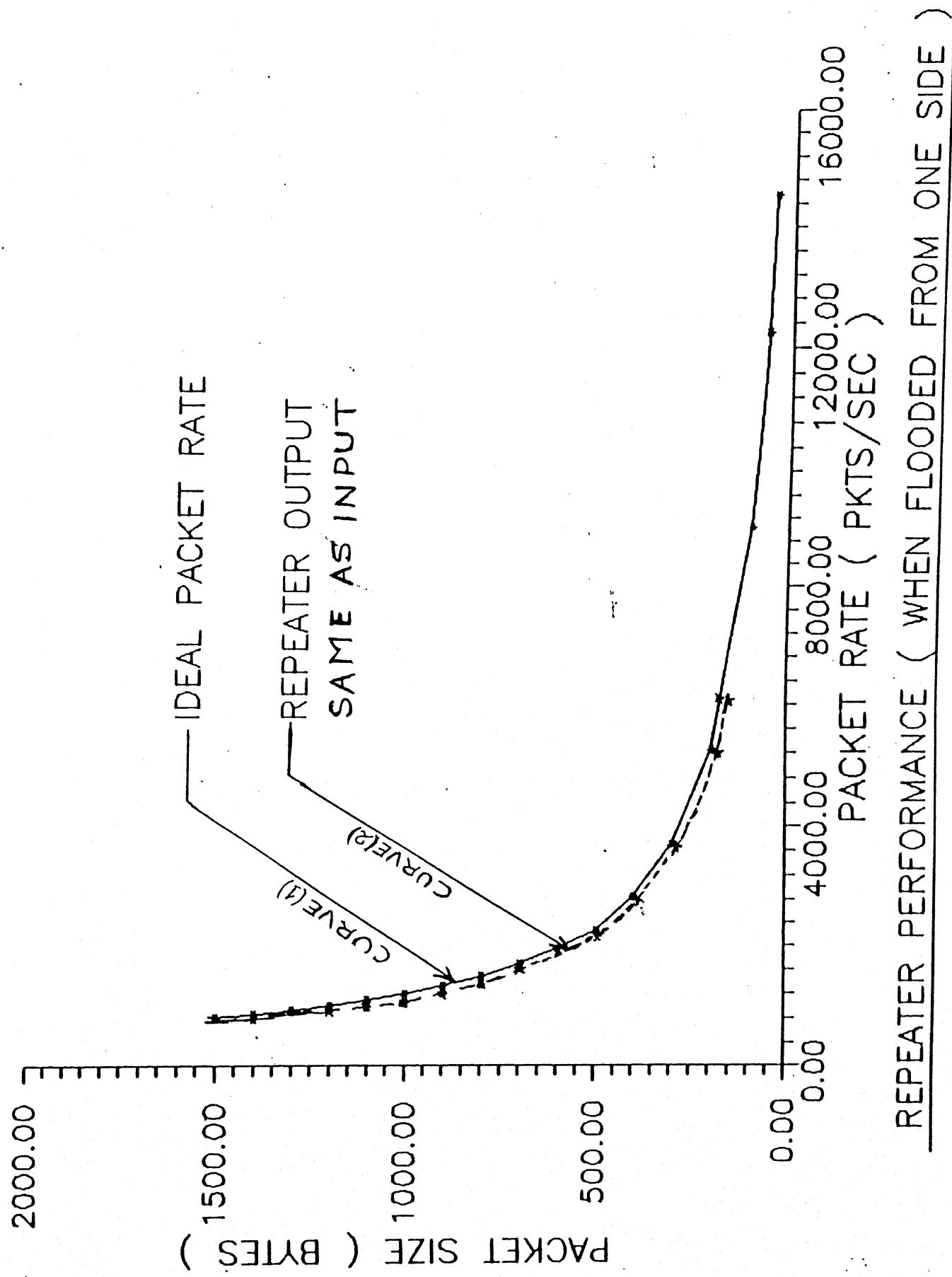
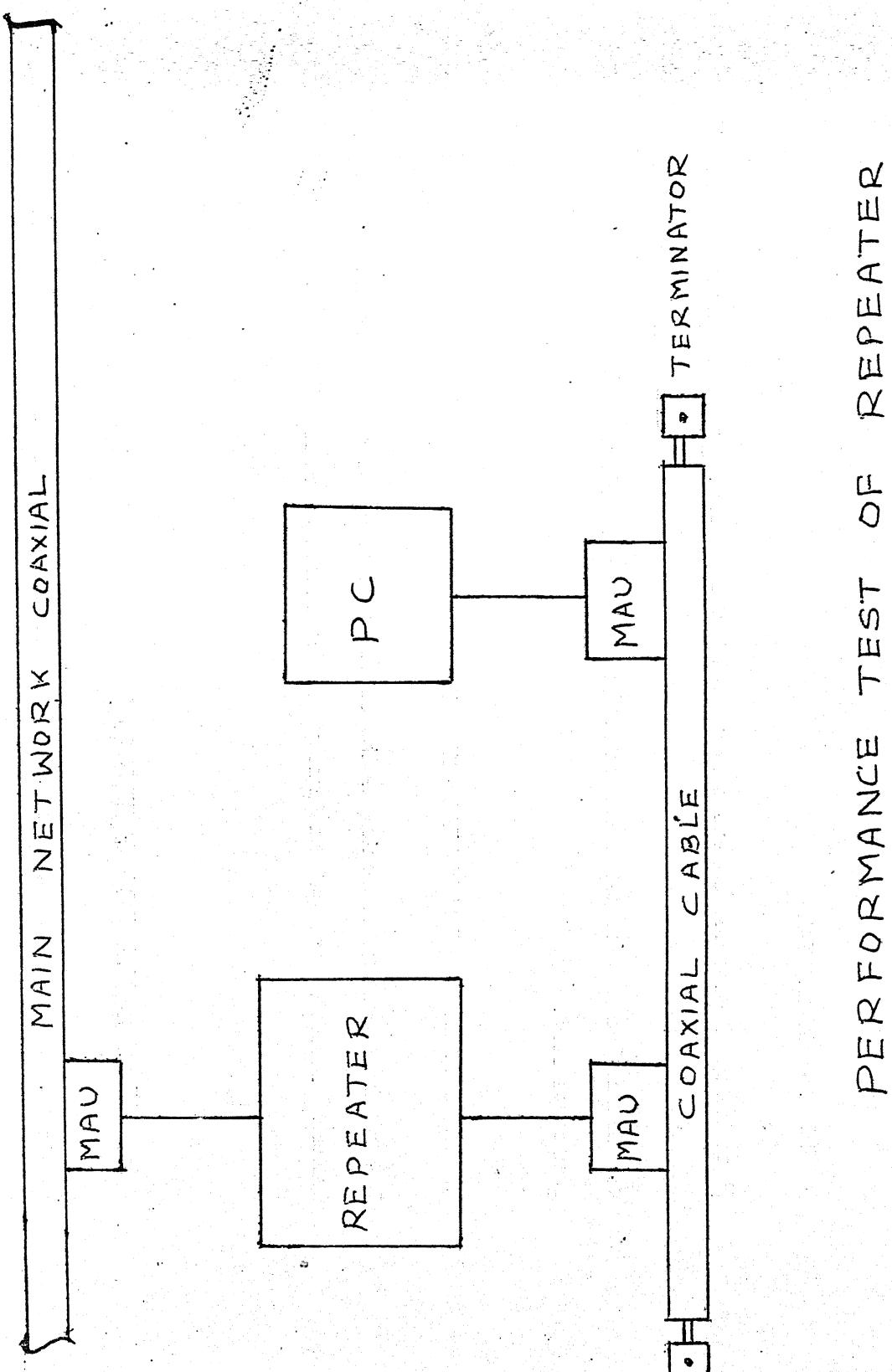


Fig 5.2



5.4 SPECIFICATIONS OF REPEATER

The specifications of this implemented Repeater can be given as follows:

1. Length of preamble bits	Minimum 56 bits
2. Packet start up delay (In to out)	7 Bits max.
3. Fragment extension	To 96 Bits
4. Collision and jam propagation delay to jam output	7 Bits max.
5. Power supply	5Vdc and 15Vdc
6. LEDs	Indicating <ul style="list-style-type: none"> 1. Power supply 2. Input at port 1. 3. Input at port 2.
7. Connectors	Two 15 pin female
8. Cable	Two AUI Ethernet
9. Size	10" * 10" * 3"
10. The Transceiver units connected to this Repeater must be without SQE Test.	

5.5 CONCLUSION

The repeater unit has been fabricated on a wirewrap board as per the preceding chapters, conforms to the IEEE 802.3 standards. The design has been simplified which was possible only due to the FIFO chip. The collision circuitry has also been simplified as NOOR pin of ESI was pulled high.

It was observed that as long as the frequencies of received clock and system generated clock of 10 MHz do not vary much the data transfer is smooth without any error. That is why the system clock was brought to a closer value of 20 MHz i.e, 20.000677 MHz.

It uses an expensive 1K size FIFO due to non availability of a smaller size FIFO. It is suggested that a minor design changes using faster small FIFO preferably 1 bit wide and 16 bit deep be made.

With the adjustment of clock frequency and fixing of components on a printed circuit board, this repeater can be a perfect working model and can be installed on main network. Even this wire wrap fabricated repeater unit behaved perfectly well on network. A power pack which can give 5 volt 1 amp dc as well as 15 volt 300 m amp dc has to be placed along with the working model to give power to repeater unit as well as to the transceiver unit to which this is to be connected.

This repeater unit can further be modified to work as a multiport repeater unit. For this a robust circuitry has to be developed for to and fro movement of data through all ports.

This repeater unit can be made an intelligent repeater by using some central processing unit which will monitor the performance of it and on line information of packet size, packet rate, no of collisions in network, no of short packets etc can be seen on a small monitor. The same can be sent to some near by monitoring station too as a normal data packet for remote monitoring.

REFERENCES

- [1] Andrew S. Tanenbaum "Computer Networks" 2nd edition Prentice Hall of India New Delhi 1990
- [2] D Bertsekas/R Gallagar "Data Networks" Prentice Hall of India New Delhi 1989
- [3] Misha Schartz "Telecommunication Networks Protocol, Modeling and Analysis" Addison-Wesley Publishing Company
- [4] ANSI/IEEE Standards 802.3, "Carrier Sense Multiple Access with Collision Detection [CSMA/CD]" Access Method and Physical Layer Specification IEEE Publication.
- [5] Microcommunications Handbook Intel Publication 1987
- [6] Cabletron Systems ST 500 Transciever [MAU] Ethernet/IEEE 802.3
- [7] Manual For Transceiver Module FN 2004-Fuzikura
- [8] Operational Manual For Fan Out Unit LN 430-387
- [9] SGS Thomson Microelectronics Manual for MK 45H02 N-35 FIFO

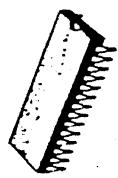
ORDERING INFORMATION

PART NO.	ACCESS TIME	R/W CYCLE TIME	CLOCK FREQ.	PACKAGE TYPE	TEMPERATURE RANGE
MK45264N-55	55 ns	75 ns	13.3 MHz	24 Pin Plastic DIP	0° to 70°C
MK45265N-55	55 ns	75 ns	13.3 MHz	24 Pin Plastic DIP	0° to 70°C
MK45264N-70	70 ns	95 ns	10.5 MHz	24 Pin Plastic DIP	0° to 70°C
MK45265N-70	70 ns	95 ns	10.5 MHz	24 Pin Plastic DIP	0° to 70°C

MK45H01/02/03(N,K)
-25/35/50/65/12

HIGH SPEED 512/1K/2K x 9
CMOS BiPORT™ FIFO

ADVANCE DATA



K
PLCC32
(Plastic Chip Carrier)

N
DIP-28
(Plastic Package)

- FIRST-IN FIRST-OUT MEMORY BASED ARCHITECTURE
- FLEXIBLE X 9 ORGANIZATIONS : MK45H01 (512 x 9), MK45H02 (1K x 9), MK45H03 (2K x 9)
- LOW POWER, HIGH SPEED HCMOS TECHNOLOGY
- ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE
- FULLY EXPANDABLE IN WORD WIDTH AND DEPTH
- EMPTY AND FULL WARNING FLAGS
- RETRANSMIT CAPABILITY
- HALF-FULL FLAG IN SINGLE DEVICE MODE

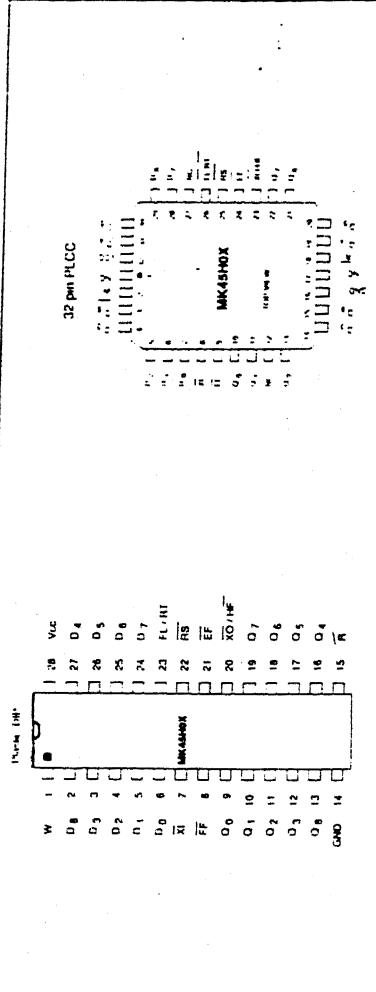
DESCRIPTION

The MK45H01, MK45H02, and MK45H03 are members of the BiPORT FIFO Family from SGS-THOMSON Microelectronics, which utilize special two-port memory cell techniques. Specifically, these devices implement a First-in-First-out (FIFO) algorithm, featuring asynchronous read/write operations, full, empty, and half full status flags, and unlimited expansion capability in both word size and depth. The full and empty flags are provided to prevent data overflow and underflow. The data is loaded and emptied on a first-in-first-out basis, and the latency for retrieval of data is approximately one load (write) cycle. These devices feature a read/write cycle time of only 35ns (28.5MHz).

PIN NAMES

\bar{W}	Write	\bar{X}_I	Expansion In
\bar{R}	Read	\bar{X}_O	Expansion Out
$\bar{R}S$	Reset	$\bar{F}F$	Full Flag
$\bar{F}L\bar{R}T$	First Load	$\bar{E}\bar{E}$	Empty Flag
	Retransmit	$\bar{H}\bar{F}$	Half-full Flag
$D_{0\,B}$	Data In	V_{cc}	Power, +5 V
$D_{0\,B}$	Data Out	GND	Ground

Figure 1: Pin Connections.



DESCRIPTION (continued)

The reads and writes are internally sequential through the use of separate read and write pointers in a ring counter fashion. Therefore, no address information is required to load or unload data. Data is loaded and unloaded with the use of W (write), and R (read) input pins. Separate data in (D0-D8) and data out (Q0-Q8) pins allow simultaneous and asynchronous read/write operations, provided the status flags are not protecting against data underflow or overflow.

The main application of these devices is a buffer for sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The MK45H01, MK45H02, and MK45H03 incorporate 9-bit wide data arrays that provide for support control or parity bit functions. This feature is helpful in data communications where the extra parity bit is used for transmission and reception error checking. These devices also offer retransmit (R) and half-full features in single device or width expansion modes. The retransmit function allows data to be re-read by resetting the read pointer while not disturbing the write pointer. This is for applications where the FIFO is not full, or is written with less than 512, 1024, or 2048 words. The MK45H01, MK45H02, and MK45H03 continue our 28-pin industry standard

FUNCTIONAL DESCRIPTION

Unlike conventional shift register based FIFOs, the MK45H01, MK45H02, and MK45H03 employ a memory-based architecture wherein a byte written into the device does not 'ripple through'. Instead, a byte written into the device is stored in a specific location, where it remains until over-written. The byte can be read and re-read as often as desired in the single device configuration.

Two internal pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illegal operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written. The address pointers automatically loop back to address zero after reaching the final address in the FIFO (512, 1024, or 2048). The empty, half full, and full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch up to another, the FIFO can be written and read continuously without ever becoming full or empty.

Unlike conventional shift register based FIFOs, the MK45H01, MK45H02, and MK45H03 employ a memory-based architecture wherein a byte written into the device does not "ripple through". Instead, a byte written into the device is stored in a specific location, where it remains until over-written. The byte can be read and re-read as often as desired in the single device configuration.

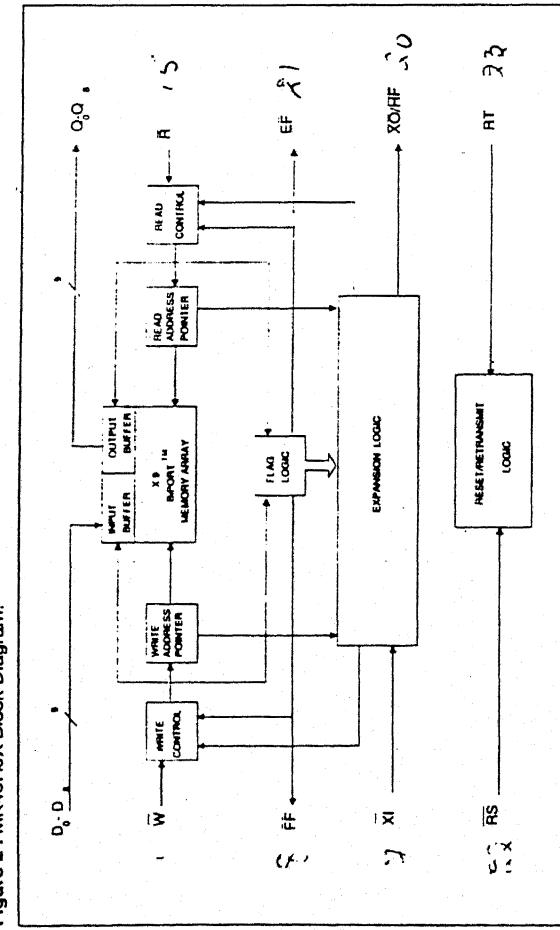
Two internal pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading, un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written. The address pointers automatically loop back to address zero after reaching the final address in the FIFO (512, 1024, or 2048). The empty, half full, and full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read one continuously without ever becoming full or empty.

ABSENTEE VOTING

Parameter	Value	Unit	mA
Voltage on any Pin (relative to Ground)	0.3 to + 7.0	V	
Operating Temperature	0 to + 70	C	
Storage Temperature	-55 to + 125	C	
Power Dissipation	1	Watt	
Output Current	20		

source and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The MK45H01, MK45H02, and MK45H03 incorporate 9-bit wide data arrays that provide for support control or parity bit functions. This feature is helpful in data communications where the extra parity bit is used for transmission and reception error checking. These devices also offer retransmit (RT) and half-full features in single device or width expansion modes. The retransmit function allows data to be read by resetting the read pointer while not disturbing the write pointer. This is for applications where the FIFO is not full, or is written with less than 512, 1024, or 2048 words. The MK45H01, MK45H02, and MK45H03 continue our 28-pin industry standard

Figure 2: Wavelengths of Siganus

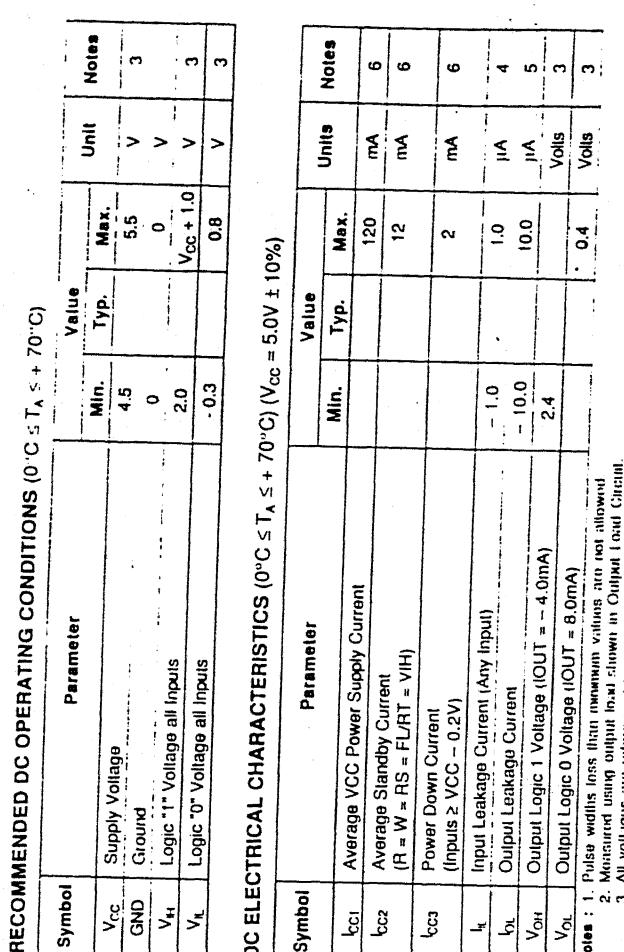


ABSENTEE VOTING

Parameter	Value	Unit	mA
Voltage on any Pin (relative to Ground)	0.3 to + 7.0	V	
Operating Temperature	0 to + 70	C	
Storage Temperature	-55 to + 125	C	
Power Dissipation	1	Watt	
Output Current	20		

sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The MK45H01, MK45H02, and MK45H03 incorporate 9-bit wide data arrays that provide for support control or parity bit functions. This feature is helpful in data communications where the extra parity bit is used for transmission and reception error checking. These devices also offer retransmit (RT) and half-full features in single device or width expansion modes. The retransmit function allows data to be read by resetting the read pointer while not disturbing the write pointer. This is for applications where the FIFO is not full, or is written with less than 512, 1024, or 2048 words. The MK45H01, MK45H02, and MK45H03 continue our 28-pin industry standard operations, such as read bytes (reading while empty) or write bytes (writing while full). Once a given address has been read, it can be addressed again automatically. The address pointers automatically dress zero after reaching the final FIFO (512, 1024, or 2048). The empty/full status of the FIFO is therefore distance between the pointers, not location. As long as the pointers do not another, the FIFO can be written continuously without ever becoming full.

supporting an 8-bit wide data at a maximum data rate of 125 Mbps. The MK45H01, MK45H02, and MK45H03 are interfacing fast processors and slow portate 9-bit wide data arrays that provide control or parity bit functions. This lead in data communications, where the extra used for transmission and reception etc. These devices also offer retransmit FIFO features in single device or wide modes. The retransmit function allows read by resetting the read pointer while the write pointer. This is for applying the FIFO is not full, or is written with less than 1024, or 1024 words. The MK45H01 and MK45H03 continue our 28-pin integrated pin-out assignment.



4. Measured with 0.4 \cdot V_{M} \cdot $V_{I,i}$
 5. $R \geq V_{in} \cdot 0.4 \cdot V_{out} \cdot V_{i,i}$
 6. Icc measurements are made with outputs open

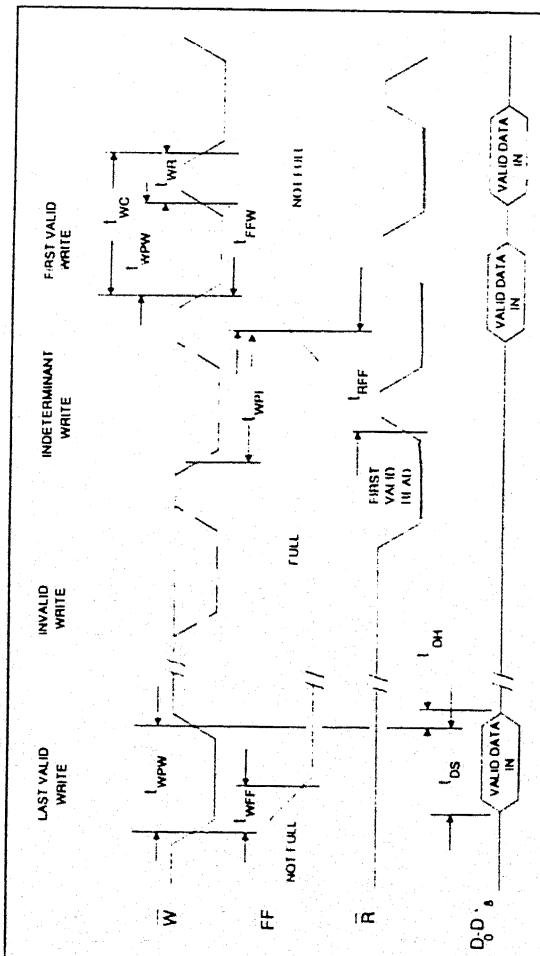
Resetting the FIFO simply resets the write and read pointers to location zero. Pulsing retransmit resets the read address pointer without effecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading individual FIFOs. The penalty of cascading is often unacceptable ripple through delays. The MK45H01, MK45H02, and MK45H03 allow implementation of very large FIFOs with no timing penalties. The memory-based architecture of the device allows connecting the read, write, data-in, and data-out lines of the device in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins.

WRITE MODE

The MK45H0X initiates a Write Cycle (see figure 3A) on the falling edge of the Write Enable control input.

Figure 3A : Write and Full Flag Timing.

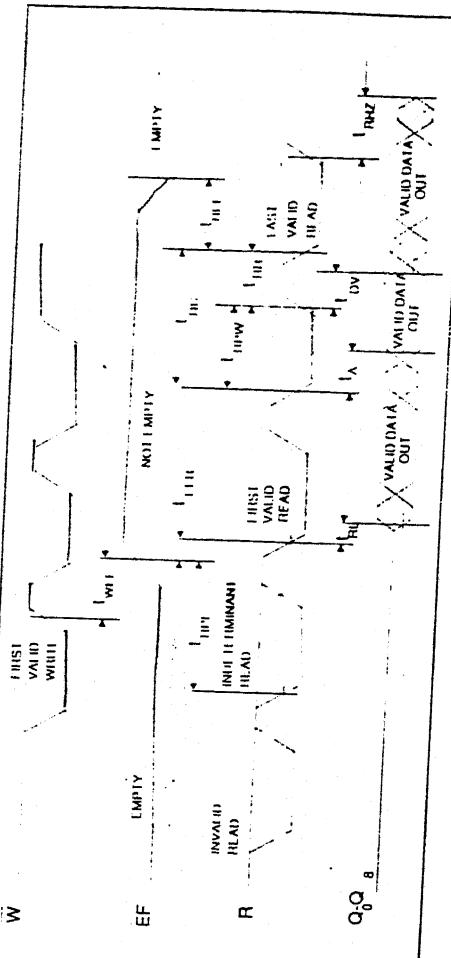


(\bar{W}) , provided that the Full Flag (\bar{FF}) is not asserted. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of W . The data is stored sequentially and independent of any ongoing Read operations. \bar{FF} is asserted during the last valid write as the MK45H0X becomes full. Write operations begun with FF low are inhibited. FF will go high (t_{FF}) after completion of a valid READ operation. FF will again go low (t_{FW}) from the beginning of a subsequent WRITE operation, provided that a second READ has not been completed (see figure 4A). Writes beginning (t_{FW}) after FF goes high are valid. Writes beginning after FF goes low and more than t_{FW} before FF goes high are invalid (ignored). Writes beginning less than t_{FW} before FF goes high and less than t_{FW} later may or may not occur (be valid), depending on internal flag status.

READ MODE

The MK45H0X initiates a Read Cycle (see figure 3B) on the falling edge of Read Enable control input (R), provided that the Empty Flag (EF) is not asserted. In the read mode of operation, the MK45H0X provides a fast access to data from 9 of the locations in the static storage array. The data is accessed on a FIFO basis independent of any ongoing WRITE operations. After R goes high, data outputs will return to a high impedance condition until the next read operation. In the event that all data has been read from the FIFO, the EF will go low, and further READ operations will be inhibited (the data inputs will remain in high impedance). EF will go high (t_{LEF}) after completion of a valid WRITE operation. EF will again go low (t_{REF}) from the beginning a subsequent read operation, provided that a second WRITE has not been completed (see figure 4B). Reads beginning (t_{REF}) after EF goes high are valid. Reads begun after EF goes high are invalid (ignored). Reads beginning less than t_{REF} before EF goes high and less than t_{REF} later may or may not occur (be valid) depending on internal flag status.

Figure 3B : Read and Empty Flag Timing.



AC ELECTRICAL CHARACTERISTICS ($0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$) ($V_{CC} = +5.0\text{V} \pm 10\%$)

Sym.	Parameter	-25			-50			-65			-120			Unit	Notes
		Min.	Max.												
I_{RC}	Read Cycle Time	35	45	65	80	140	140	120	120	ns	ns				
I_{RA}	Access Time	25	~	35	50	65	65	20	20	ns	ns				
I_{RF}	Read Recovery Time	10	10	15	15	20	20	ns	ns						
I_{RPW}	Read Pulse Width	25	35	50	65	120	120	ns	ns						
I_{RL}	\bar{R} Low to Low Z	0	0	0	0	0	0	ns	ns						
I_{RV}	Data Valid from \bar{R} High	5	5	5	5	5	5	ns	ns						
I_{RHZ}	\bar{R} High to High Z	18	20	25	25	35	35	ns	ns						
I_{RFZ}	\bar{R} Low to \bar{EF} Low	30	35	40	60	60	60	ns	ns						
I_{ERF}	\bar{EF} High to Valid Read	10	10	10	10	10	10	ns	ns						
I_{WFZ}	\bar{W} High to \bar{EF} High	30	35	45	60	60	60	ns	ns						
I_{RPi}	Read Protect indeterminate	10	10	10	10	10	10	ns	ns						

Figure 4A : Read/Write to Full Flag.

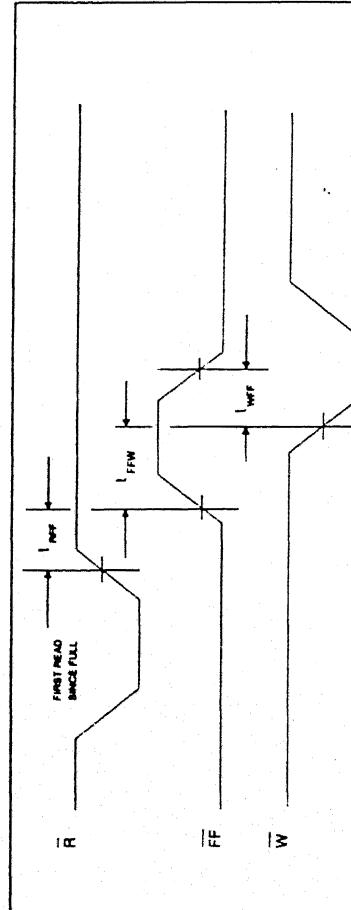
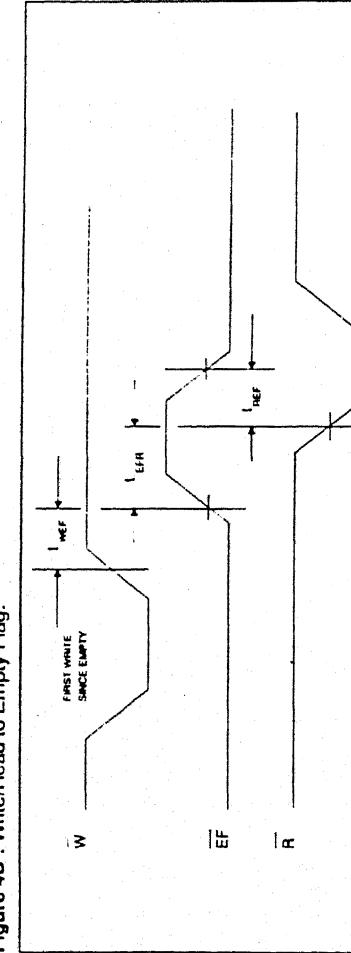


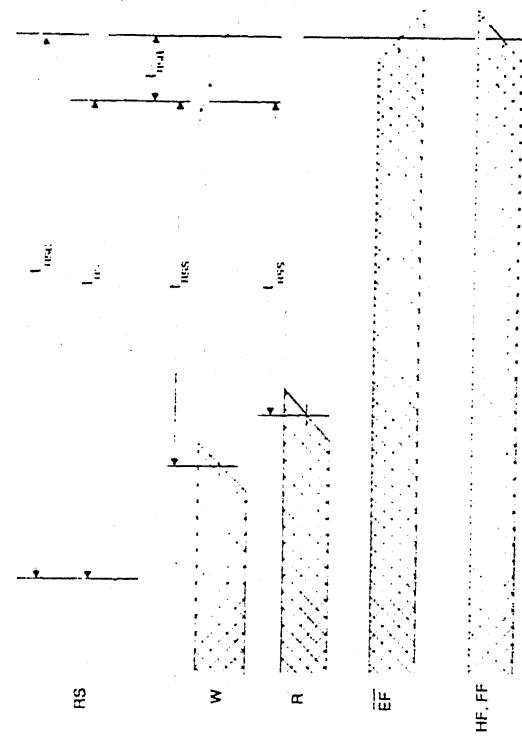
Figure 4B : Write/Read to Empty Flag.



RESET

Although neither \bar{W} or \bar{R} need be high when \bar{RS} goes low, both R and W must be high (less before RS goes high, and must remain high (less afterwards. Refer to the following discussion for the required state of \bar{FLRT} and \bar{XI} during Reset.

Figure 5 : Reset.



Note : HF, EF and FF may change status during Reset, but flags will be valid at t_{RS} .

AC ELECTRICAL CHARACTERISTICS ($0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$) ($V_{CC} = +5.0\text{V} \pm 10\%$)

Sym.	Parameter	-25			-35			-50			-65			-120			Unit	Notes
		Min.	Max.															
t_{RC}	Reset Cycle Time	35	45	45	65	65	65	80	80	140	140	65	80	140	140	ns		
t_{RS}	Reset Pulse Width	25	~	35	35	35	35	50	50	120	120	65	65	120	120	ns		
t_{RR}	Reset Recovery Time	10	10	10	15	15	15	15	15	ns	ns	15	15	20	20	ns		
t_{RSS}	Reset Set Up Time	25	~	30	30	30	30	45	45	100	100	45	45	100	100	ns		

